TR4P133AT/AF General Purpose Micro-controller

1. General Descriptions

The TR4P133AT/AF series are a high-performance 4-bit RISC micro-controller embedded with 2KX12 bits OTP, 32X4 bits SRAM, 14 I/O pins (12 I/O pins and two input pins). it's flexible and cost-effective solution for general purpose MCU applications.

2. Features

- MCU Operating voltage: 1.8V to 3.6V
- MCU Operation frequency:
  (a) Use Internal 32MHz RC OSC : MCU run at 0.25MIPS/1 MIPS /2 MIPS /4 MIPS
  (b) Use External XTOSC: MCU run at 0.5 MIPS (1MHz x'tal) ~8 MIPS (16MHz x'tal).
- Memory Size
  - Program ROM size: 2KX12 bits (OTP type)
  SRAM size: 32x4 bits
- Wake up function for power-down mode
  - HALT mode wake up source: RTC timer overflow or PA0~3, PB0~3, PD0~3 and PC0~PC1 edge trigger.
- Provided 12 input /output pins: each I/O has bit programmable as input or output port, these 12 I/Os also provided edge trigger wake up function and pull up resistors configured by registers.
  (a) They are provided with high sink current 20mA @VDD=3V, VOL=0.5V.
  (b) They are provided with drive current 7mA @VDD=3V, VOH=2.5V.
  (c) Pull up 150k ohm resistor.
- Provided 1 input pin (PA3), shared with RESETB/VPP pin by option, pull up 150k ohm resistor and edge trigger wake up function.
- Provided 1 input pin (PC1), with pull up 150k ohm resistor and edge trigger wake up function.
- One 8 bits timer, clock source of timer is F_{MCK} /8192(or 4096,2048,1024), the content of timer can be cleared and read by program, it can be used as RTC timer when 32K X'tal oscillator mode is enabled.
- Oscillator type by option
  (a) External X'tal oscillator 1~16MHz or 32KHz (external ceramic resonator or crystal oscillator, the pin of X'tal is shared with PB0 and PB1 pin)
  (b) Built-in internal RC OSC 32 MHz ----
  frequency deviation within ± 2%, VDD=1.8V~3.6V, temp= -20 ºC ~70 ºC
- Four reset condition
  - Low voltage reset (LVR=1.55V)
  - Power on RC-reset
  - External reset (RSTB) pin shared with PA3 by option.
  - Watch dog timer overflow reset (WDT period is 0.524 Sec~4.192 Sec, if MCU run at 4MIPS)

Selection table

Feature / P/N	TR4P133AT	TR4P133AF
Real OTP PROM size	**1.6K words (1536 x 12 + 48X12)**	**2K words (1984 X 12)**
User Information block (Note 1)	**Yes**	**No**
reusable COB by UV erasing	**No**	**Yes**
SRAM	**32 x 4 bits**	
I/O Pins	**12 I/O and 2 Input PIN**	

Note 1 : Support user Information block (48X12 bits) for serial number , lot number or programmable optional codes … etc., it's locate at address 640h ~ 66Fh.

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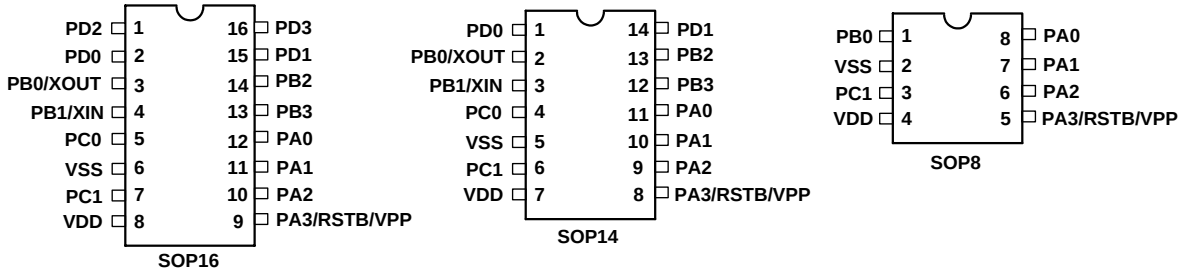
Package SOP14/SOP16 /SOP8



.Pads Information

PAD Name	Type	State After Reset	Description
Reset/Power Input			
VDD	P	High	Power input pin.
VSS	P	Low	Ground input pin.
General I/O ports			
PA0~PA2	I/O	XXXX	PA0~PA2 are programmable bi-direction pin. Pull up resistor 150k ohm. It's provided level changed wake up function.
PA3/VPP (RSTB)	I	X	PA3 is a shared pin with external reset RSTB pin by option. Pull up resistor 150k ohm. PA3 is also as VPP pin, no option is needed. It's provided level changed wake up function.
PB0/XOUT /OSCADJ	I/O	X	PB0 is a programmable bi-direction pin. Pull up resistor 150k ohm. PB0 is shared with XOUT/OSCADJ by option. It's provided level changed wake up function. PB1/XIN and PB0/XOUT connected to external X'tal (1~16MHz or 32KHz) PB0/OSCADJ pin is the frequency adjust pin of HRCOSC.
PB1/ XIN	I/O	X	PB1 is a programmable bi-direction pin. Pull up resistor 150k ohm. PB1 is shared with XIN pin by option. It's provided level changed wake up function.
PB2~PB3	I/O	XX	PB2, PB3 is a programmable bi-direction pin. Pull up resistor 150k ohm. It's provided level changed wake up function.
PC0	I/O	X	PC0 is a programmable bi-direction pin. Pull up resistor 150k ohm. It's provided level changed wake up function.
PC1	I	X	PC1 is an input pin with pull up resistor 150k ohm and level changed wake up function.
PD0~PD3	I/O	XXXX	PD0 ~ PD3 are a programmable Input /Output port. Pull up resistor 150k ohm. It's provided level changed wake up function.

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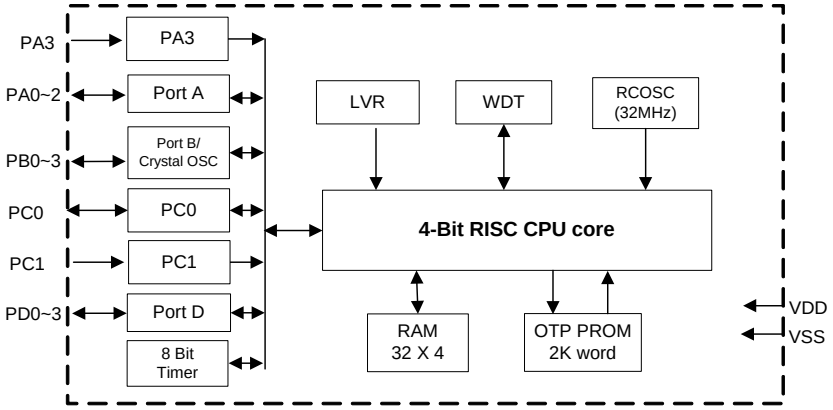
Block Diagram



4. ELECTRICAL CHARACTERISTICS

4.1 Absolute Maximum Ratings

ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYSMBOL	RATING	UNIT
DC Supply Voltage	V+	< 7.0	V
Input Voltage Range	V_{IN}	-0.5 to VDD+0.5	V
Operating Temperature	T_A	-40 to 85	ºC
Storage Temperature	T_{STO}	-50 to 150	ºC

4.2 DC/AC Characteristics

DC CHARACTERISTICS (TA = 25℃, VDD = 3V, unless otherwise noted)

PARAMETER	SYMBOL	TEST CONDITIONS	LIMIT			UNIT
			Min	Typ	Max	
Operating voltage	V_{DD}	-	1.8	-	3.6	V
Operating Current	I_{OP1}	3V , MCU run at 4 MIPS	-	1.7	-	mA
Standby Current 1	I_{STBY1}	MCU stop, WDT off	-	0.1		uA
Standby Current 2	I_{STBY2}	MCU stop, WDT off, 32K x'tal OSC. on	-	1.7	3	uA
Input High Level	V_{IH}	All I/O port	0.8*V_{DD}	-	-	V
Input Low Level	V_{IL}	All I/O port	-	-	0.2*V_{DD}	V
Input Resistor	R_{up}	Pull up 150K ohm	-	150	-	K ohm
Output Drive Current	I_{OH}	VDD=3V , V_{OH}=2.5V	-	-7	-	mA
Output Sink Current	I_{OL1}	VDD=3V , V_{OL}=0.5V	-	20	-	mA
LVR	V_{LVR}			1.5		V

AC CHARACTERISTICS (TA = 25℃, VDD = 3V, unless otherwise noted)

PARAMETER	SYMBOL	TEST CONDITIONS	LIMIT			UNIT
			Min	Typ	Max	
Internal HRCOSC Frequency	F_{OSC1}	VDD=1.8V~3.6V Temp.= -20 ºC ~70 ºC	31.36	32 ±2%	32.64	MHz

External XTOSC	F_{XTOSC}	VDD=1.8V~3.6V		1~16MHz or 32KHz		M/KHz
MCU Operation frequency	F_{MCK1}	VDD=1.8V~3.6V Use HRCOSC		4/2/1/0.25		MHz
	F_{MCK2}	VDD=1.8V~3.6V Use XTOSC		8~0.5		MHz
MCU Operation voltage	V_{OP}		1.8	3.0	3.6	V
WDT period	T_{WDT}	VDD=1.8V~3.6V		If F_{MCK}=4MHz (1)(2^21)/F_{MCK} =0.524 (2)(2^22)/F_{MCK} =1.048 (3)(2^23)/F_{MCK} =2.096 (4)(2^24)/F_{MCK} =4.192		Sec
Stable clock delay after power on or system reset	CKstable1	(Note 1)	-	320us + 1024 x (1/ F_{MCK}) (Note 2)		us
Stable clock delay after wake up	CKstable2	System oscillator --HRCOSC (Note 3)	-	64 x (1/ F_{MCK}) (Note 2)		us
Stable clock delay after wake up	CKstable3	System oscillator --XTOSC (Note 4)	-	1024 x (1/ F_{MCK}) (Note 2)		us

Note1: The stable clock delay (CKstable 1) is place after first clock output of HRCOSC or external X'tal before user's first instruction, it means the user's program will get more stable clock after power on reset.

Note2: F_{MCK} = MCU operating clock F_{MCK1} or F_{MCK2}.

Note3: The stable clock delay (CKstable 2) is place after first clock output of HRCOSC before user's first instruction, it means the user's program will get more stable clock after wake up.

Note4: The stable clock delay (CKstable 3) is place after first clock output of external X'tal before user's first instruction, it means the user's program will get more stable clock after wake up.

5. FUNCTIONAL DESCRIPTION

This MCU inside TR4P133AT/AF is a high performance process, and operation frequency could be from 0.25 MIPS up to 4MIPS depending on the application.

5.1 Program ROM (PROM)

TR4P133A series supports two szie OTP PROM, they are TR4P133AT and TR4P133AF. The OTP PROM memory plan is shown below:

Address	TR4P133AT (1.6 K OTP PROM)	TR4P133AF (2 K OTP PROM)
000h ~ 0FFh	User area 1.5K (1536 X12)	User area 1.5K (1536 X12)
100h ~ 1FFh		
200h ~ 2FFh		
…..		
500h ~ 5FFh		
600h ~ 63Fh	Reserved area	Reserved area
640h ~ 66Fh	User Information block(48X12), only for data storing only, don't use to store program	User area 0.5K (448X12)
670h ~ 7FFh	Reserved area	

5.2 SRAM and I/O Memory Map

TR4P133AT/AF provided 32 nibbles SRAM on the locations $20H~$3FH, these address of SRAM is different from PROM's address.

Direct Addressing (use MAH)		Real SRAM Address	SRAM MAP
MAH=XH (MAH no effect)	00H~1FH		Common I/O port and SFR(special function register) register
MAH=0H	20H~3FH	00H~1FH	USER SRAM (32x4)

5.3 Halt Mode & Wake up

The MCU is changed into HALT mode (MCU clock and HRCOSC stop) when HALT instruction is executed. It provides a power saving mode for those applications requiring a very low stand-by current. The PA0~PA3, PB0~PB3, PD0~PD3, PC0 and PC1 are provided the wake up function when rising edge or falling edge trigger occurred in halt mode. The program counter will be changed to $004H when HALT instruction executed immediately, and program counter will go to next address after stable time delay (CKstable2/3, see page 4) while wake up condition occurred. "System Resetb" signal will release HALT state and execute reset procedure because reset is first priority when in HALT mode, so program counter will be changed from $004h to $000h, program counter goes to next address after stable time delay (CKstable1, see page 4). Furthermore, the SRAM will keep their previous data without changed in this mode.

5.4 Watch Dog Timer Reset (WDT)

The watch dog timer (WDT) is used to reset whole chip when detect unexpected execution sequence caused by accident condition, avoiding dead lock of MCU program. This timer can be enabled or disabled by option. WDT will not have any action when WDT disabled. Software shall run an "clear watch dog timer" (write data 5h to register $1D) instruction before WDT time out if WDT is enabled. Hardware will generate a reset signal to reset whole system when WDT overflow. The watch dog timer is a simple counter. If the operating frequency of MCU is 4MIPS, it's provided four kinds of time-out period (0.524 Sec~4.192 Sec) by WDTS1 and WDTS0 option, and the clock source uses internal HRCOSC oscillator. WDT can works in NORMAL mode but disabled in HALT mode, because the clock source come from internal HRCOSC oscillator.

5.5 Programable 8 bits TIMER1

The Timer 1 is an 8 bit up timer. The overflow interval can be easy generated by reading the content value of timer 1 and reset values of Timer 1 to 00h by setting TIM1EN=0. The content value of Timer 1 would be readable only by programmer. The interrupt isn't provided in TR4P133 series, using polling TM1FG is the only way to check out the overflow of Timer1.

Use external 32K X'tal oscillator for RTC timer

The clock source of Timer1 can be optioned by XT32ENB to built a RTC timer, and MCU still run at 0.25MIPS,1 MIPS,2 MIPS or 4 MIPS. If XT32ENB option is enabled, PB0 and PB1 pin must be connected to 32KHz X'tal, it's only a clock source of timer1 for RTC timer, the RTC period can be set by T1DIV1 and T1DIV0 registers as shown in table below:

F_{32K} = External X'tal 32KHz clock

T1DIV1	T1DIV0	RTC time period
0	0	1/(F_{32K} /32768)=1S
0	1	1/(F_{32K} /16384)=0.5S
1	0	1/(F_{32K} /128)=3.906ms
1	1	1/(F_{32K} /32)=0.976ms

If TM1EN is set to high, The timer1 overflow flag (TM1FG) will be set to high when RTC time period overflow, and the RTC timer can be cleared by TM1EN setting to 0 if need. Using polling TM1FG is the only way to check out the overflow of RTC in normal mode, and MCU will be wake up when RTC overflow in halt mode.

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5.6 Reset

The “system resetb” signal is combined with four signals, they are power on reset, low voltage reset (LVR), external RSTB pin and WDT overflow reset. A dedicated RSTB pin is provided to reset this chip by external. For normal operation of this chip, a good RSTB is needed. This pin provided built-in 150K ohm pull up resistor. The MCU will go back to NORMAL mode when RSTB occurred in HALT mode.

5.7 Low Voltage Reset

When VDD power is applied to the chip, the low voltage RSTB default is enabled initially, it will be disabled when in halt mode. The internal system RSTB will be generated if VDD power below about V_{LVR}(1.5V).

5.7 System Clock Oscillator

The TR4P133AT/AF is provided internal high speed RC oscillator (HRCOSC) and external X’tal oscillator or ceramic resonator (XTOSC) for many application requirements.

Condition VDD=1.8V~3.6V

TYPE	OSC frequency	MCU clock (F_{MCK})
HRCOSC	(1) 32MHz ±2%	F_{HRCOSC} / 8 /16 /32 / 128 MCU run at 4 MIPS/ 2 MIPS / 1 MIPS / 0.25MIPS
	(2) 32MHz -15%~+15% by PB0/OSCADJ pin serial with resistor to VDD or VSS	
	(3) 32KHz crystal for RTC	
XTOSC	1MHz~16MHz crystal	F_{XTOSC} / 2 /4 /8 /16 if use 4MHz crystal MCU run at 2MIPS/ 1MIPS / 0.5MIPS / 0.25MIPS

5.9 I/O Port

This chip provided total 12 I/O ports, they are bi-direction I/O port PA0~PA2, PB0~PB3, PD0~PD3 and PC0, the I/O ports provided with input and output direction controlled by IOC_PA, IOC_PB, IOC_PD and IOCPC0, and all I/O also provided wake up and pull up resistor function by control register.

5.9.1 Port A /Port B (input/output)

The Port A and Port B are 4-bit I/O port except PA3 is an input port. They can be bit programmable setting as input port or output port. In output mode, the data can be written out to external pin by DATA_PA OR DATA_PB register, and reading this output port will get data from DATA_PA or DATA_PB register. Pull-up resistor (150K ohm) will be disabled when output mode is selected.

In input mode, Port A and Port B data can be read from external pin by reading DATA_PA or DATA_PB register, and they are provided pull-up resistor 150K or not by PAPU, PBPU registers.

In addition, each pin of Port A and Port B also can be with wake up function by using register PAWK or PBWK setting to 1. In HALT mode, If Port A or Port B with wake up enabled by these registers, any edge trigger (rising or falling) occurred on Port A or Port B will wake up system and turn on HRCOSC or XTOSC oscillator, and the program counter of MCU will jump to the address 04H, running the wake up sub-routing program.

PA3 is an input pin only, provided with pull up 150K ohm and edge wake up function. It’s shared with external reset pin (RSTB) pin by option, and VPP pin.

PB0 is shared with XOUT/OSCADJ by option and PB1 is shared with XIN pin by option. These XIN and XOUT PIN can be connected to external X’tal to replace internal oscillator HRCOSC. Once XTENB option is enabled, the pull up control registers and I/O direction registers of these PINs will be disabled by hardware automatically.

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5.9.2 Port C (Output)

PC0 is an bi-direction I/O port and it can be set as input port or output port by IOCPC0 register. In addition, it also provided edge trigger (rising or falling) wake up function and pull up resistor.
PC1 is an input port, it also provided edge trigger (rising or falling) wake up function and pull up resistor.

5.9.3 Port D (input/output)

Whether all 4 bits of the Port D is input or output port depends on IOC_PD control register.
Port D also provided edge trigger (rising or falling) wake up and pull up resistor 150K, function just like Port A or Port B

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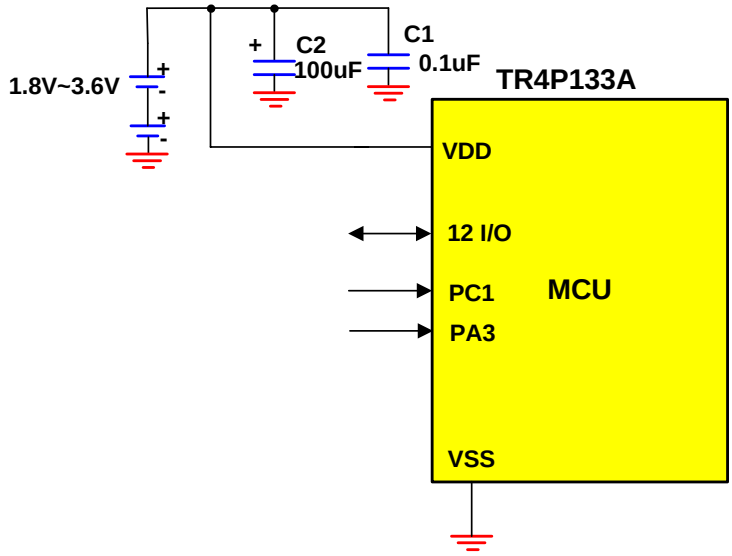
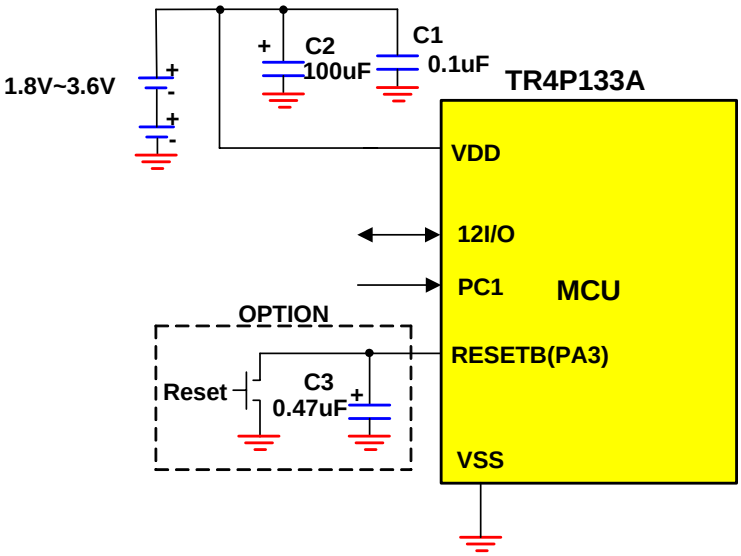
6. Application Circuit



Note : Substrate must be connected to VSS.



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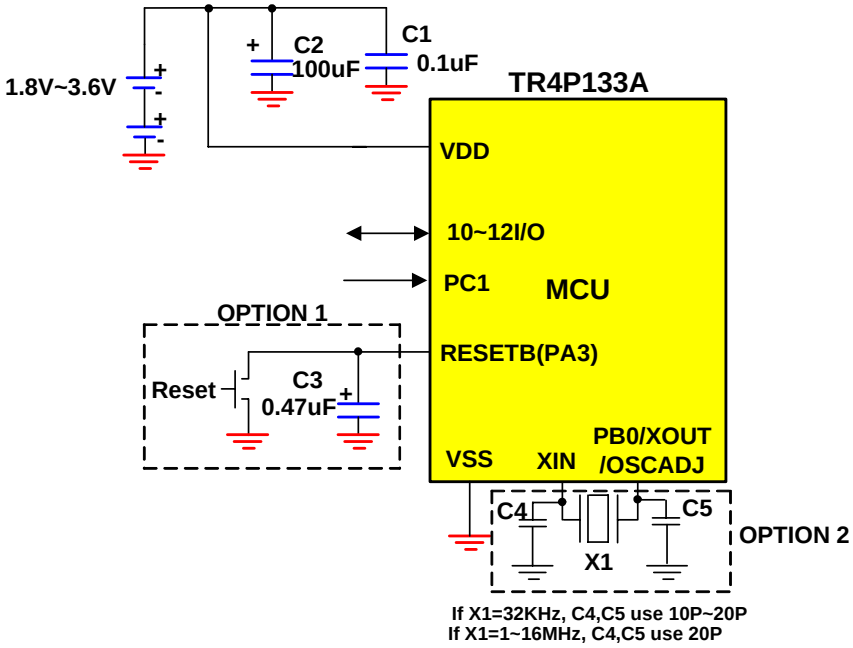
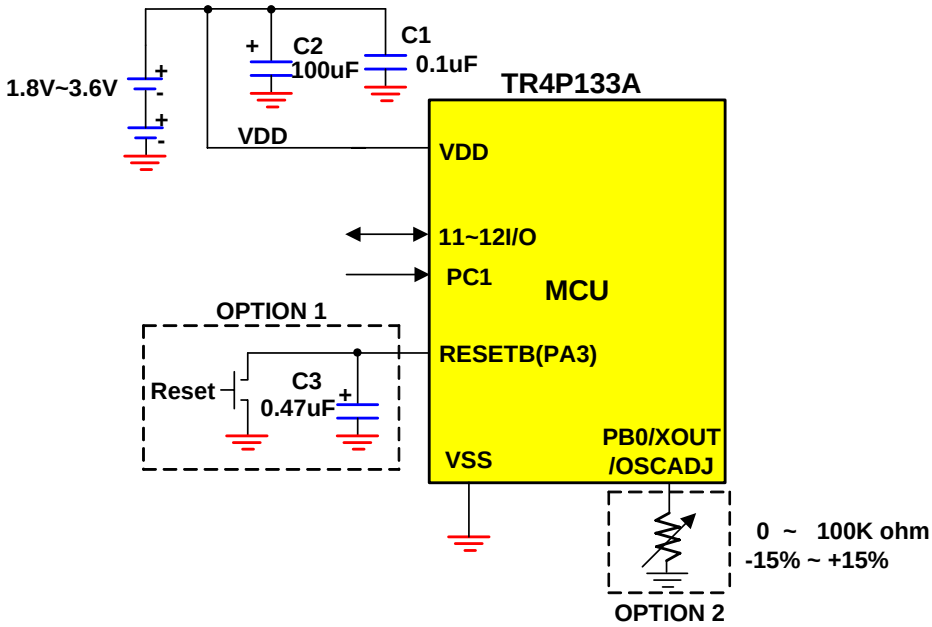


Note : Substrate must be connected to VSS.



Note : Substrate must be connected to VSS.

7. Internal Option Registers

<table>
<tr><th>Option Name</th><th>Function Description</th></tr>
<tr><td>WDTEN</td><td>WDT enabled/disabled control</td></tr>
<tr><td>PA3_RSTB</td><td>PA3 pin shared with RSTB pin enabled/disabled control</td></tr>
<tr><td>XTENB</td><td>External crystal mode enabled/disabled control</td></tr>
<tr><td>OADJENB</td><td>PB0 is a shared pin with OSCADJ PIN (Adj. pin of HRCOSC) enabled/disabled control</td></tr>
<tr><td>MCKS1
MCKS0</td><td>MCU operating clock definition (external crystal frequency= F_{XTOSC})
<table>
<tr><th>Select</th><th>Option XTENB=1
Use internal HRCOSC</th><th>Option XTENB=0
Use external XTOSC (F_{XTOSC})</th></tr>
<tr><td>0</td><td>MCU run at 0.25MIPS</td><td>MCU run at F_{XTOSC} /16 MIPS</td></tr>
<tr><td>1</td><td>MCU run at 1MIPS</td><td>MCU run at F_{XTOSC} /8 MIPS</td></tr>
<tr><td>2</td><td>MCU run at 2MIPS</td><td>MCU run at F_{XTOSC} /4 MIPS</td></tr>
<tr><td>3</td><td>MCU run at 4MIPS</td><td>MCU run at F_{XTOSC} /2 MIPS</td></tr>
</table></td></tr>
<tr><td>XT32ENB</td><td>32K X’tal oscillator enabled/disabled control</td></tr>
</table>

8. Revision History

Version	Description	Page	Date
1.0	Established		Jul, 28 2011
1.1	1. (1) 2KX12 bits (2) RTC timer overflow or PA0~3, PB0~3, PD0~3 and… (3) 32K X’tal oscillator (4) clock source of timer is F_{MCK} /8192(or 4096,2048,1024) (5) 1MHz~4MHz or 32KHz (6) LVR=1.55V	P1	Sep, 02 2011
	2. block diagram	P3	
	3. F_{XTOSC} /2 = 0.5~8	P5	
	4.(1) Hardware will generate a reset (2) WDTS1 and WDTS0 option (2) because the clock source come from internal HRCOSC oscillator. (3) The clock source of	P6	
	5. Once XTENB option is enabled, the pull up control registers …	P7	
	6. Application circuit , If X1=32KHz, C2,C3 use 10P~20P	P9	
1.2	1. (1) MCU run at 0.5 MIPS (1MHz x’tal) ~8 MIPS (16MHz x’tal) (2) and PC0~PC1 edge trigger. (3) if MCU run at 4MIPS (4) Support user Information block (48X12 bits)	P1	Sep,20 2011
	2. Pad information	P2	
	3. (1) from 0.25 MIPS up to 8 MIPS (2) WDT period (3) program counter goes to next address after stable time delay (CKstable1)	P4	
	4. and MCU still run at 0.25MIPS,1 MIPS,2 MIPS or 4 MIPS	P5	
	5. they are power on reset, low voltage reset	P6	
	6. (1) MCU run at 4 MIPS/ 2 MIPS / 1 MIPS / 0.25MIPS (2) MCU run at 2MIPS/ 1MIPS / 0.5MIPS / 0.25MIPS	P6	
	7. MCU operating clock definition	P10	

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