TR4P271AT/AF ADC Type Micro-controller

1. General Descriptions

The TR4P271A series are a high-performance 4-bit RISC micro-controller(MCU) embedded with 2KX12 bits OTP, 256X4 bits SRAM, on chip temperature sensor ,up to 6 channel 12 bit ADC, up to 3 channel 10 bit PWM with 6 I/O outputs, Bandgap reference voltage for low battery detector, 11 Input/Output ports and one input port, it's flexible and cost-effective solution for industrial control products, household appliances, consumer products, motor control applications, etc.

2. Features

- Operating voltage:
  (A) MCU run 14 KIPS ~ 8 MIPS
  (1) 1.7V to 5.5V for Temp. = 25℃
  (2) 2.0V to 5.5V for Temp. = -40℃~+85℃
  (B) MCU run 10 MIPS ~ 16 MIPS
  (1) 2.3V to 5.5V for Temp. = 25℃
  (2) 2.5V to 5.5V for Temp. = -40℃~+85℃

- These MCU can operate in high speed. Oscillator type can be selected by option setting. High speed and low speed operating mode is selectable by software. Below is the chip performance in different modes.
  (a) Internal high speed HRCOSC: 16 MIPS / 8 MIPS / 4 MIPS / 1 MIPS or low speed LRCOSC 114.69KIPS (thousand instructions per second) / 57.34 KIPS / 28.67 KIPS / 14.33 KIPS.
  (b) External EXTOSC: 16 MIPS (32 MHz X'tal) ~ 227.5KIPS (455 KHz X'tal).
- Up to 8 level stacks for call sub-routing.
- Memory Size
  - Program ROM size : 2KX12 bits (OTP type)
  - SRAM size: Total 256x4 bits SRAM
- Up to 6 channel 12 bit ADC
- Up to 3 channel 10 bit PWM function.
- Wake up function for power-down mode
  - HALT Mode wake up source: RTC timer overflow, PA0~3, PB0~3 and PD0~3 edge trigger
- 11 input /output pins: PA0~PA2, PB0~PB3, PD0~PD3 each I/O has bit programmable as input or output port, these 11 I/Os also provided level changed wake up function, pull up/down resistor configured by register.
- 1 input port PA3, PA3 is shared with RSTB (reset) pin by option. It also provides level-change-wakeup function. Pull up and pull down resistor can be configured by software too.
- Port A, Port B and Port D are provided with high sink current 24mA @VDD=5V,Vol =0.5V(except PA3)
- Port A, Port B and Port D are provided with high drive current 23mA @VDD=5V,Voh=4.5V(except PA3)
- PA1 built-in 38KHz modulator by option.
- One Op-Amp is provided, three pins shared with PD0, PD1, PB2 (by option).
- One comparator is provided, two input pins shared with PD2, PD3 (by option).
- Three timers
  - Timer 1: 10 bits timer/counter/PWM, its clock source can be from chip-internal or external.
  - Timer 2: 8 bits timer
  - RTC : time period 0.125 /0.25/0.5/1 Sec or 15.625/31.25/62.5/125 ms,
    RTC Clock source comes from internal LRCOSC or external 32K X'tal.
- Four reset condition
  - Low voltage reset (LVR 1.7V~2.8V by option)
  - Power on reset
  - External RSTB pin is shared with PA3 pin by option.
  - Watch dog timer overflow reset (0.125 sec ~ 1 sec by option)

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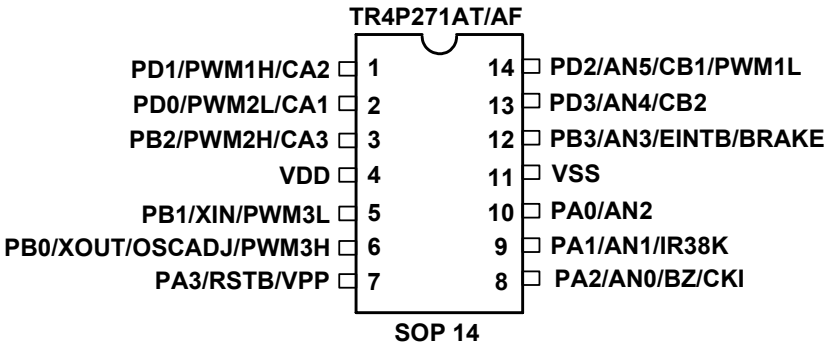
- Four internal interrupt sources, ADC, TIMER1, TIMER2, RTC interrupt.
- WDT(Watch dog timer)
  - □ WDT can be enabled/disabled in HALT Mode by option
  - □ WDT clock source comes from internal LRCOSC or external 32K X'tal for reliable operation.
- Built-in external X'tal oscillator (EXTOSC), suitable for 455KHz~32MHz external ceramic resonator or crystal oscillator, crystal pins are shared with PB1 and PB0 by option.
- Built-in high frequency internal 32MHz RC OSC (HRCOSC, frequency deviation within ±2%, temperature range at -40℃~+85℃, VDD = 2.0V to 5.5V)
- Built-in low frequency internal RC OSC (LRCOSC) 459KHz (frequency deviation within ±12%)
- One external interrupt EINTB PIN (PB3 pin).
- Support on chip temperature sensor, temperature range: -40°C ~ 85 °C. (accuracy about ± 6°C)
- Bandgap reference voltage for low battery detector

Package (14/16 SOP)



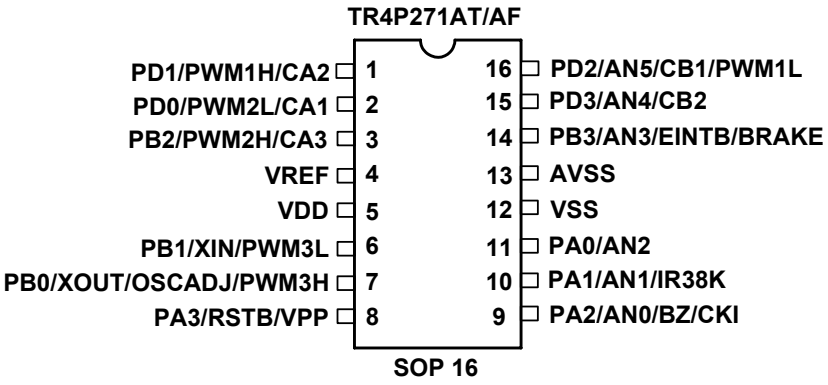


Figure 1 14/16 SOP package

3. Pads Information

PAD Name	Type	Reset	Description
Power Input			
VDD	I	High	Power input pin
VSS	I	Low	Ground input pin
AVSS	I	Low	Analog circuit ground input pin
General I/O ports			
PA0 (AN2)	I/O	X	PA0 is a programmable I/O port, with pull up/down resistor 100K ohm. Level change wake up function is provided. PA0 is shared with AN2 by option
PA1 (AN1/IR38K)	I/O	X	PA1 is a programmable I/O port, with pull up/down resistor 100K ohm. Level change wake up function is provided. PA1 is shared with AN1 or IR38K by option
PA2 (AN0/BZ/CKI)	I/O	X	PA2 is a programmable I/O port, with pull up/down resistor 100K ohm. Level change wake up function is provided. PA2 is shared with AN0,BZ or CKI by option
PA3 (RSTB/VPP)	I	X	PA3 is an input pin with pull up resistor 60K, pull down 100K ohm. Level change wake up function is provided. PA3 is shared with VPP pin or RSTB pin (external reset) by option
PB0 (XOUT/OSCADJ/ PWM3H)	I/O	X	PB0 is a programmable I/O port, with pull up/down resistor 100K ohm. Level change wake up function is provided. PB0 is shared with XOUT, OSCADJ or PWM3H by option. XIN and XOUT is connected to external X'tal. OSCADJ pin is used for frequency adjust of HRCOSC.
PB1 (XIN/PWM3L)	I/O	X	PB1 is a programmable I/O port, with pull up/down resistor 100K ohm. Level change wake up function is provided PB1 is shared with XIN or PWM3L pin by option. XIN is connected to external X'tal 32K or 455KHz~32MHz.
PB2 (PWM2H/CA3)	I/O	X	PB2 is a programmable I/O port, with pull up/down resistor 100K ohm. Level change wake up function is provided. PB2 is shared with PWM2H or CA3 by option. CA3 is an output of the OP Amp.
PB3/ (AN3/EINTB/ BRAKE)	I/O	X	PB3 is a programmable I/O port, with pull up/down resistor 100K ohm. Level change wake up function is provided PB3 is shared with AN3, EINTB or BRAKE by option.
PD0 (PWM2L/CA1)	I/O	X	PD0 is a programmable I/O port, with pull up/down resistor 100K ohm. Level change wake up function is provided PD0 is shared with PWM2L or CA1 by option. CA1 is a positive input of the OP Amp.
PD1 (PWM1H/BZ/ CA2)	I/O	X	PD1 is a programmable I/O port, with pull up/down resistor 100K ohm. Level change wake up function is provided. PD1 is shared with PWM1H, BZ or CA2 by option. CA2 is a negative input of the OP Amp.
PD2 (AN5/ PWM1L CB1)	I/O	X	PD2 is a programmable I/O port, with pull up/down resistor 100K ohm. Level change wake up function is provided. PD2 is shared with AN5, PWM1L or CB1 by option. CB1 is a positive input of the comparator.
PD3 (AN4/CB2)	I/O	X	PD3 is a programmable I/O port, with pull up/down resistor 100K ohm. Level change wake up function is provided. PD3 is shared with AN4 or CB2 by option. CB2 is a negative input of the comparator.
VREF	I	X	External reference voltage input for ADC

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Block Diagram

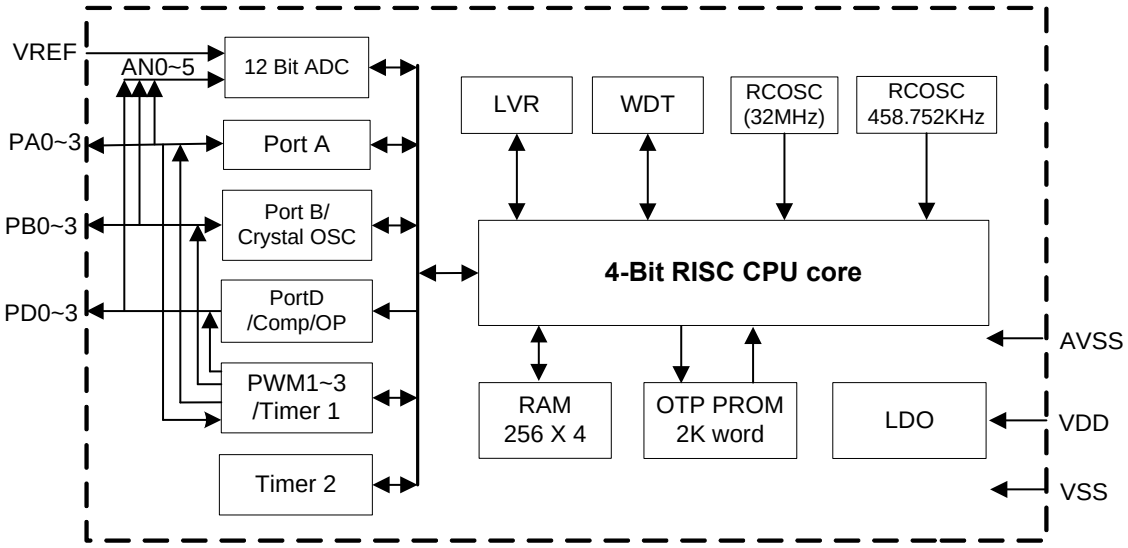

Figure 2 Block Diagram

4. ELECTRICAL CHARACTERISTICS

4.1 Absolute Maximum Ratings

ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYSMBOL	RATING	UNIT
DC Supply Voltage	V+	< 7.0	V
Input Voltage Range	V_{IN}	-0.5 to VDD+0.5	V
Operating Temperature	T_A	-40 to +85	ºC
Storage Temperature	T_{STO}	-50 to +150	ºC

4.2 DC/AC Characteristics

DC CHARACTERISTICS (TA = 25℃, VDD = 3V, unless otherwise noted)

PARAMETER	SYMBOL	TEST CONDITIONS	LIMIT			UNIT
			Min	Typ	Max	
Operating voltage	V_{VDD1}	Temp.= -40℃~+85℃ MCU run 14KIPS~ 8 MIPS	2.0 (V_{LVR2})		5.5	V
	V_{VDD2}	Temp.= -40℃~+85℃ MCU run 10 MIPS~16MIPS	2.5		5.5	V
Operating Current	I_{OP1}	VDD=3V , MCU run 16 MIPS		3.6		mA
	I_{OP2}	VDD=5V , MCU run 16 MIPS		4.0		mA
	I_{OP3}	VDD=3V , MCU run 1 MIPS		1.6		mA
	I_{OP4}	VDD=5V , MCU run 1 MIPS		1.9		mA
	I_{OP5}	VDD=3V , MCU run 14KIPS		30		μA
Standby Current	I_{STBY1}	MCU stop in HALT Mode WDT & RTC off		2.5 (VDD=3V) 3 (VDD=5V)		μA
	$I_{STBY2\_}$	1.VDD=5V 2.MCU stop in HALT Mode, WDT on or RTC on		8		μA
	$I_{STBY3\_}$	1.VDD=5V 2.RTC clock source is EXT32K 3.MCU stop in HALT Mode, RTC on		8		μA
Input High Level	V_{IH}	All I/O port	0.8*V_{DD}			V
Input Low Level	V_{IL}	All I/O port			0.2*V_{DD}	V
Output Drive Current	I_{OH1}	VDD=3V , V_{OH}=2.5V,All I/O port	-8	-15		mA
	I_{OH2}	VDD=5V , V_{OH}=4.5V,All I/O port	-12	-23		mA
Output Sink Current	I_{OL1}	VDD=3V , V_{OL}=0.5V,All I/O port	8	15		mA
	I_{OL2}	VDD=5V , V_{OL}=0.5V,All I/O port	12	24		mA
PA,PB,PD pull down Res.	R_{down1}	Pull down 180K ohm, VDD=3V	140	180	220	K ohm
	R_{down2}	Pull down 100K ohm, VDD=5V	60	90	120	K ohm
PA,PB,PD pull up Res. (except PA3)	R_{up1}	Pull up 180K ohm, VDD=3V	140	180	220	K ohm
	R_{up2}	Pull up 100K ohm, VDD=5V	60	90	120	K ohm
PA3 pull up Res.	R_{up3}	Pull up 60K ohm ,VDD=2V~5V	40	60	80	K ohm
LVR	V_{LVR1}	Temp. = 25℃	1.5	1.7	1.9	V
	V_{LVR2}	Temp.= -40℃~+85℃	1.4	1.7	2.0	V
RAM Data Retention	V_{DR}		1.4			V

AC CHARACTERISTICS (TA = 25℃, VDD = 3V, unless otherwise noted)

PARAMETER	SYMBOL	TEST CONDITIONS	LIMIT			UNIT
			Min	Typ	Max	
Internal HRCOSC Frequency	F_{HRCOSC}	VDD = 2.0V~5.5V Temp = -40℃~+85℃	31.36	32 ±2%	32.64	MHz
Internal LRCOSC Frequency	$F_{LRCOSC1}$	VDD = 2.0V~5.5V Temp. = 25℃		458.752 ±12%		KHz
	$F_{LRCOSC2}$	VDD = 2.0V~5.5V Temp = -40℃~+85℃		458.752 ±20%		KHz
External X'tal EXTOSC	F_{XTOSC}	VDD = 2.0V~5.5V		1~32		MHz
External X'tal EXT32K	F_{XT32K}	VDD = 2.0V~5.5V		32768		Hz
MCU operating frequency (clock source from F_{HRCOSC} or F_{XTOSC})	F_{MCk1}	1.in NORMAL Mode 2.clock source : F_{HRCOSC} 3.VDD = 2.0V~5.5V 4.Temp. -40℃~+85℃		16 ±2%, 8 ±2% 4 ±2%, 1 ±2% (F_{HRCOSC}/2, F_{HRCOSC} /4, F_{HRCOSC} /8, F_{HRCOSC} /32)		MIPS
	F_{MCk2}	1.in NORMAL Mode 2.clock source : F_{XTOSC} 3.VDD = 2.0V~5.5V 4 Temp. -40℃~+85℃ 5.If F_{XTOSC} = 32Mhz		16 , 8, 4, 1 (F_{XTOSC}/2, F_{XTOSC}/4, F_{XTOSC}/8, F_{XTOSC}/32)		MIPS
MCU operating frequency (clock source F_{LRCOSC})	F_{MCk3}	1.in GREEN Mode 2.VDD = 2.0V~5.5V 3.Temp. = 25℃		114.69±12%,57.34±12% 28.67±12%,14.33±12%		KIPS
PA1 38KHz output (clock source F_{HRCOSC} or F_{XTOSC})	F_{38K1}	1.in NORMAL Mode 2.PA1 IR38K option enabled 3.Register F38K=1 4.Temp. = 25℃		38.09 ±2% (F_{HRCOSC} /840) 38.09 (F_{XTOSC}=16Mhz)/420		KHz
PA1 38KHz output (clock source F_{LRCOSC})	F_{38K2}	1.in GREEN Mode 2.PA1 IR38K option enabled 3.Register F38K=1 4.Temp. = 25℃		38.23 ±12% (F_{LRCOSC}/12)		KHz
RTC period	T_{RTC1}	VDD = 2.0V~5.5V Temp. = 25℃ clock source F_{LRCOSC} SPUP option enabled		0.125±12%, 0.25±12% 0.5±12%, 1.0±12%		Sec
	T_{RTC2}	VDD = 2.0V~5.5V Temp. = 25℃ clock source F_{LRCOSC} SPUP option disabled		15.625±12%,31.25±12% 62.5±12%, 125±12%		ms
	T_{RTC3}	VDD = 2.0V~5.5V clock source F_{XT32K} SPUP option enabled		0.125, 0.25, 0.5, 1.0		Sec
	T_{RTC4}	VDD = 2.0V~5.5V clock source F_{XT32K} SPUP option disabled		15.625, 31.25, 62.5, 125		ms
WDT period	T_{WDT1}	VDD = 2.0V~5.5V Temp. = 25℃ clock source F_{LRCOSC}		0.125±12%, 0.25±12% 0.5±12% , 1.0±12%		Sec
	T_{WDT2}	VDD = 2.0V~5.5V clock source F_{XT32K}		0.125, 0.25, 0.5, 1.0		Sec
Bandgap reference voltage start-up time	Tbg		100			μs

Stable clock delay after power on or system reset	CKstable1 (Note 1)	System oscillator –HRCOSC F_{MCK1} < = 8 MIPS		1280 x (1/ 8MHz) + 1024 x (1/ F_{MCK1})		µs
		System oscillator --HRCOSC F_{MCK1} > 8 MIPS		1280 x (1/8MHz) + 32768 x (1/ F_{MCK1})		
	CKstable2 (Note 2)	System oscillator –XTOSC F_{MCK2} < = 8 MIPS		1280 x (1/ 8MHz) + 1024 x (1/ F_{MCK2})		µs
		System oscillator --XTOSC F_{MCK2} > 8 MIPS		1280 x (1/ 8MHz) + 32768 x (1/ F_{MCK2})		
Stable clock delay after wake up	CKstable3 (Note 3)	System oscillator --HRCOSC		64 x (1/ 8MHz)		µs
	CKstable4 (Note 4)	System oscillator --XTOSC		1024 x (1/ F_{MCK2})		µs

Note1: The stable clock delay (CKstable1) is place after first clock output of HRCOSC before user's first instruction, it means the user's program will get more stable clock after power on or system reset.
Note2: The stable clock delay (CKstable2) is place after first clock output of XTOSC before user's first instruction, it means the user's program will get more stable clock after power on or system reset.
Note3: The stable clock delay (CKstable3) is place after first clock output of HRCOSC before user's first instruction, it means the user's program will get more stable clock after wake up.
Note4: The stable clock delay (CKstable4) is place after first clock output of XTOSC before user's first instruction, it means the user's program will get more stable clock after wake up.
Note5: F_{MCK1} and F_{MCK2} are MCU operating clock.

12bit ADC Characteristics
(TA = 25℃, VDD = 2.4V~5.5V, VREF = 2.4V~5.5V, Temp. -40℃ ~ +85℃, unless otherwise noted)

PARAMETER	SYMBOL	TEST CONDITIONS	LIMIT			UNIT
			Min	Typ	Max	
ADC start-up time	T_{AD_STB}			50X (1/F_{ADC})		µs
ADC operating current	I_{ADC}			0.6		mA
ADC clock frequency	F_{ADC}				4	MHz
Sampling rate	F_{SAMPLE}				256	K/sec
Differential Nonlinearity	DNL	VDD=3.4V, VREF=3.4V Sampling rate =31.25K		±1		LSB
Integral Nonlinearity	INL		±1	±2		LSB
Offset error	OS			±1		LSB
No Missing Code	NMC			10	12	Bits

OP Characteristics (TA = 25℃, VDD = 2V~5.5V, Temp. -40℃ ~ +85℃, unless otherwise noted)

PARAMETER	SYMBOL	TEST CONDITIONS	LIMIT			UNIT
			Min	Typ	Max	
Quiescent current	I_{QUI}	VDD = 2V~5.5V	30	50	70	µA
Input voltage range	V_{IN}		0		VDD	V
Output voltage range	V_{OUT}		0.1		VDD-0.1	V
Offset voltage	V_{OS}		10		100	mV
Output sink current	I_{SINK}		15		30	µA
Output source current	I_{SOU}		150		300	µA
Output resistor load	R_L		100K			Ohm

Comparator Characteristics
(TA = 25℃, VDD = 2V~5.5V, Temp. -40℃ ~ +85℃, unless otherwise noted)

PARAMETER	SYMBOL	TEST CONDITIONS	LIMIT			UNIT
			Min	Typ	Max	
Quiescent current	I_{QUI}	VDD = 2V~5.5V	1		2	μA
Input voltage range	V_{IN}		0		VDD	V
Offset voltage	V_{OS}		10		100	mV

Bandgap Characteristics
(TA = 25℃, VDD = 2.4V~5.5V, Temp. -40℃ ~ +85℃, unless otherwise noted)

PARAMETER	SYMBOL	TEST CONDITIONS	LIMIT			UNIT
			Min	Typ	Max	
Quiescent current	I_{QUI}	VDD = 5.5V		30		μA
Bandgap start-up time	T_{STUP}		100			μs
Output voltage	V_{OUT1}	VDD =2.4V~ 5.5V	0	1.175		V
Temp. coefficient	C_{TCO1}	VDD = 2.4V		53		ppm/℃
	C_{TCO2}	VDD = 5.5V		36		
Output voltage offset	V_{OUT2}	VDD =2.4V~ 5.5V Temp. -40℃~+85℃ Process variation including			±4	%

Temperature sensor Characteristics
(TA = 25℃, VDD = 2.4V~5.5V, Temp. -40℃ ~ +85℃, unless otherwise noted)

PARAMETER	SYMBOL	TEST CONDITIONS	LIMIT			UNIT
			Min	Typ	Max	
Operating current	Isen	VDD = 5.5V		210		μA
Accuracy	L_1			±6		°C
Slope	S_1	12bitADC output < TCV*		3.3		LSB/°C
	S_2	12bitADC output > TCV*		2.8		

*Note: TCV=Temperature Calibration Value at 30°C. For more detail description please see section 5.18.2.

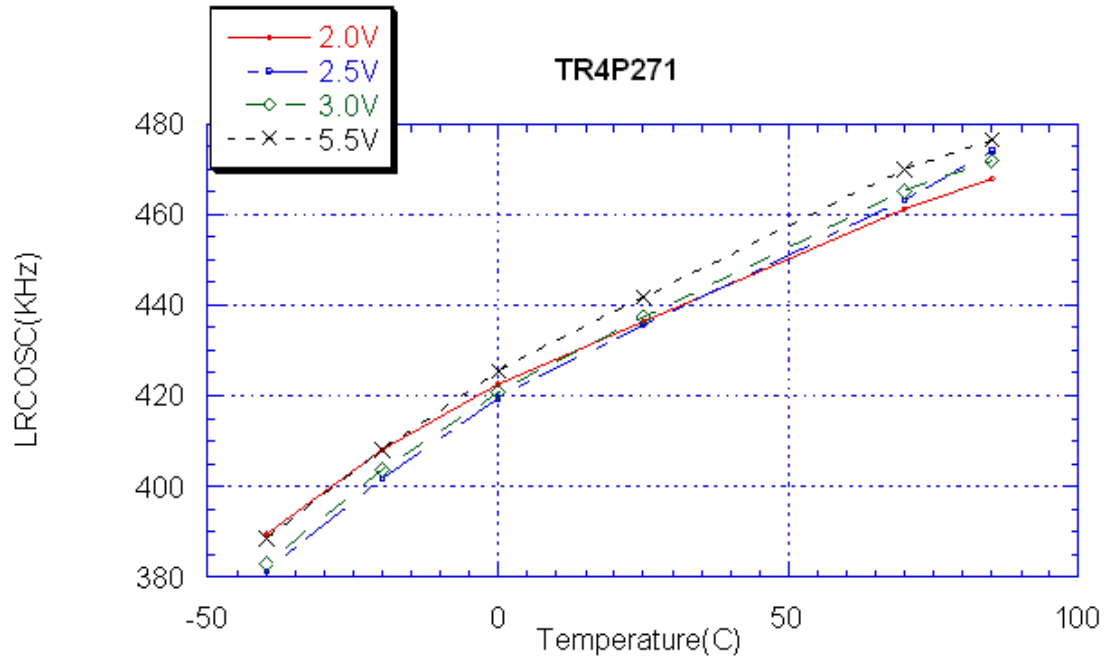

Figure 3. The LRCOSC frequency VS. temperature, VDD=2.0V~5.5V

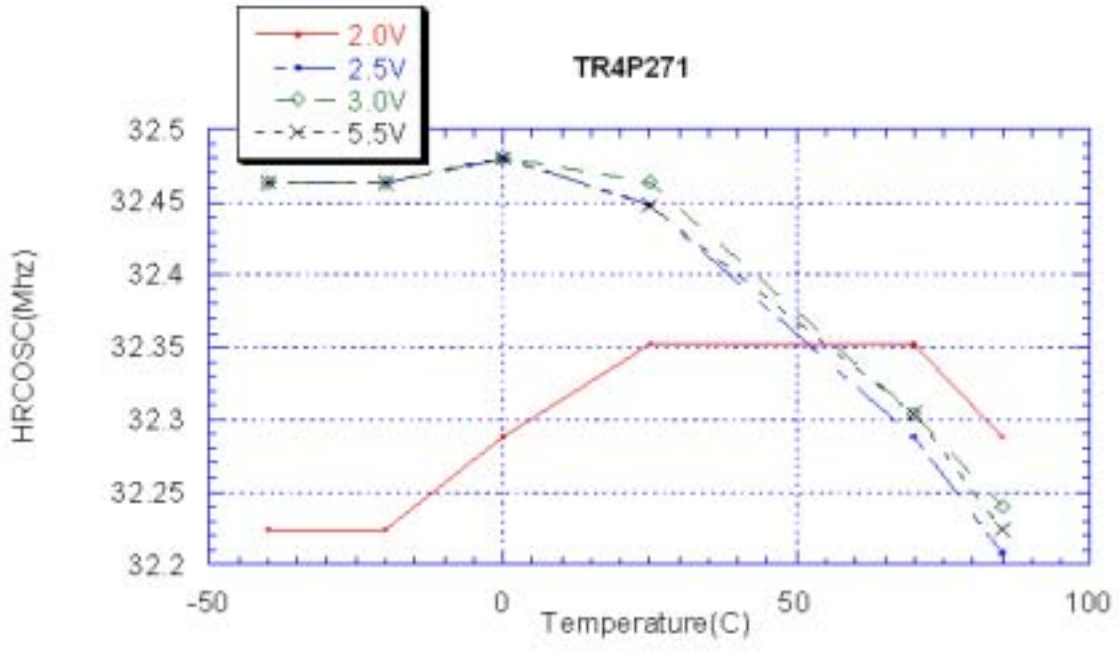

Figure 4. The HRCOSC frequency VS. temperature, VDD=2.0V~5.5V

5. FUNCTIONAL DESCRIPTION

This MCU inside TR4P271AT/AF is a high performance process, and operation frequency could be up to 16MHz depending on the application.

5.1 Program ROM (OTP PROM)

TR4P271A series support two kind of OTP ROM arrangement. They are TR4P271AT and TR4P271AF. The OTP ROM memory plan is as shown below:

Address	TR4P271AT (1.6 K OTP PROM)	TR4P271AF (2 K OTP PROM)
000h ~ 0FFh	User area 1.5K (1536 X12)	User area 1.5K (1536 X12)
100h ~ 1FFh		
200h ~ 2FFh		
…..		
500h ~ 5FFh		
600h ~ 63Fh	Reserved area (ADC calibration data & option)	Reserved area (ADC calibration data & option)
640h ~ 66Fh	User Information block(48X12), for data storing only, don't use to store program	User area 0.5K (448X12)
670h	Temperature Calibration Value (TCV)	
671h ~ 7FFh	Reserved area	

Note: 1. For TR4P271AT and TR4P271AF, the content of OTP ROM Address $640h~$66Fh can be read by program. Address $600h~$63Fh and $671h~$7FFh can't be read by program.

2. To read registers DMDL, DMDM and DMDH, only LD A,(n) instruction can be used. Other instructions are not allowed. (n= DMDL, DMDM or DMDH)

3. If DMA2~DMA0 pointed Address is located at invalid Address 600h~61Fh or 700h~7FFh, DMA2.2, DMA2.1, DMA2.0 will be automatically regarded as 0 by hardware, DMA0 and DMA1 will not be affected.

TR4P271AT supports 1.6 K words user ROM which is located on $000h ~ $5FFh, $640h ~ $66Fh and $670h. The first user area $000h ~ $5FFh stores user program area. The second user area $640h ~ $66Fh that named user information block stores serial number, lot number or user optional codes…etc. The third user area $670h stores Temperature Calibration Value. In addition to the above points, there are still the reserved areas. They are located at $600h ~ $63Fh and $671h ~ $7FFh, they can't be read by software.

TR4P271AF supports 2 K words OTP ROM which is located on $000h ~ $5FFh and $640h ~ $7FFh. These two areas store user program. Although $640h~$7FFh is user area, but data in $671h~$7FFh can't be read by software. The reserved area, $600h ~ $63Fh, can't be read by program also.

To read OTP ROM data, use DMA2~DMA0 registers as Address pointer. The Address range is located in $000H ~ $5FFH and $640H~$670H. After these registers (DMA0~2) are specified by software, the 12bits data of ROM can be moved to A register by three instructions, they are "LD A, (DMDL)", "LD A, (DMDM)" and "LD A, (DMDH)". The three instructions mentioned above are two cycle instruction, all others instructions are single cycle instruction.

Symbol	Addr.	R/W	Reset	D3	D2	D1	D0	Description
DMA0	18H	R/W	xxxx	DMA0.3	DMA0.2	DMA0.1	DMA0.0	DMA0~DMA2(exclude DMA2.3) build a 11
DMA1	19H	R/W	xxxx	DMA1.3	DMA1.2	DMA1.1	DMA1.0	bit Addressing space for read ROM data.

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DMA2	1AH	R/W	xxxx	DMA2.3	DMA2.2	DMA2.1	DMA2.0	DMA0 is the lowest nibble Address, DMA2 is the highest nibble Address. DMA2.3: It's a user usable register only, it's useless for Address setting.
DMDL	1CH	R	xxxx	DMDL.3	DMDL.2	DMDL.1	DMDL.0	DMDL is used to read low nibble data from ROM that Addressed by DMA0 ~ DMA2.
DMDM	1DH	R/W	xxxx	DMDM.3	DMDM.2	DMDM.1	DMDM.0	(1) DMDM is used to read middle nibble data from ROM that Addressed by DMA0 ~ DMA2. (2) Write this register with data 05h will clear watch dog timer (WDT) (3) Write this register with data 0Ah will clear RTC counter.
DMDH	1EH	R	xxxx	DMDH.3	DMDH.2	DMDH.1	DMDH.0	DMDH is used to read high nibble data from ROM that Addressed by DMA0 ~ DMA2.

For example, assume the data of Address 356H is 587H.

```
LD A, #3
LD (DMA2), A
LD A, #5
LD (DMA1), A
LD A, #6
LD (DMA0), A    ; ROM Address = 356H
LD A, (DMDL)    ; A register = 7H; low nibble data of ROM Address 356H
LD A, (DMDM)    ; A register = 8H; middle nibble data of ROM Address 356H
LD A, (DMDH)    ; A register = 5H; high nibble data of ROM Address 356H
        .......
```

5.2 SRAM and I/O Memory Map

TR4P271AT/AF provides 256 nibbles SRAM. SRAM is separated into 8 pages (MAH0~7). Every page has 32 nibbles (with same Address, $20H~$3FH). This Addressing space of SRAM is different from ROM's Address.

Direct Addressing (use MAH)		**Real SRAM Address**	**SRAM MAP**
MAH=XH (MAH no effect)	**00H~1FH**		Common I/O port and SFR(special function register) register
MAH=0H	**20H~3FH**	00H~1FH	USER SRAM (256x4)
MAH=1H	**20H~3FH**	20H~3FH	
|	|	|	
MAH=6H	**20H~3FH**	C0H~DFH	
MAH=7H	**20H~3FH**	E0H~FFH	

The Addressing space is separated into several pages. Software can select working pages by setting MAH register. Each page contains two blocks and each block contains 32 nibbles. The lower block (00H ~1FH) is used for IO registers and special registers, it's named "common I/O block". This block will not affected by MAH setting. In any MAH setting, software can access register of this block directly. The higher block (20H~3FH) is used for user SRAM access. MAH register determines current access page of SRAM. The 20H~3FH Address(in instructions) determines 32 nibble Address in the current page.

The working space is as shown below:

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High 32 nibbles Address space (20 ~ 3F H), MAH pointed SRAM space
Low 32 nibbles Address space (0 ~ 1F H), I/O and special register, “common I/O block”, MAH has no effect on this block

MAH = 0 selects 1st 32 nibbles SRAM
MAH = 1 selects 2nd 32 nibbles SRAM
MAH = 2 selects 3rd 32 nibbles SRAM
...
etc.
MAH can be written by a special instruction "LDMAH" with direct data.
MAH can’t be read by MCU. When interrupt happened, MAH data will be stored by hardware and restored by "RETI" command.

5.3 I/O Memory Map

The I/O memory map consists of common I/O, control registers and extended I/O space. Detailed operations are as follows.

5.4 Common I/O and control register

The "common IO block" contains 32 Addresses. All registers in this block can be accessed directly by these instructions : LD/ADC/SBC/OR/AND/XOR/INC/DEC/RLC/RRC/CMP/ADR. SET, CLR (bit set/clear) can only operate on the Address range from 00H to 0FH.
Read common I/O instruction: LD/ADC/SBC/CMP/OR/AND/XOR (Ex. LD A,(n))
Write data to common I/O instruction: LD (n),A
Read and write common I/O instruction : DEC/INC/ADR/RRC/RLC (Ex. DEC (n))

5.3 I/O Memory Map

The I/O memory map consists of common I/O and extended I/O. These I/O provide some data operation instructions as follows:
U: unchanged X: unknown value R/W: readable & writeable R: readable only W: writeable only

Symbol	Addr.	R/W	Reset	D3	D2	D1	D0	Description
STATUS	00H	R/W	00xx	TM2IFG	TM1IFG	CF	ZF	ZF : Zero status register CF : Carry status register TM1IFG: Timer 1 interrupt flag 0: no Timer1 interrupt occurred. 1: Timer1 interrupt occurred, it can be cleared by software. TM2IFG: Timer 2 interrupt flag 0: no Timer 2 interrupt occurred. 1: Timer2 interrupt occurred, it can be cleared by software.
RTC	01H	R/W	0000	RTCFG	F38K	RTCS1	RTCS0	RTC will cause an interrupt ($008h) when in NORMAL mode or GREEN mode. In HALT mode, RTC can wake up MCU and program will go to wake up vector ($004h). RTCS1, RTCS0: RTC interrupt period detailed description in Real Time Clock Interrupt section. F38K is valid only when IREN is enabled. F38K = 1, PA1 output 38k clock F38K = 0, PA1 PIN 38K output signal disabled. PA1 keeps low if (option) IRNOR0 disabled. PA1

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								keeps high when IRNOR0 enabled. RTCFG: RTC overflow flag 0: RTC overflow not occurred. 1: RTC overflow occurred, it can be cleared by software.
IOC_PA	02H	R/W	0000	X	IOCA2	IOCA1	IOCA0	Port PA0~PA2 input/output direction : 1: set port as output port individually 0: set port as input port individually PA3 is input only.
DATA_PA	03H	R/W	xxxx	DPA3 (Read only)	DPA2	DPA1	DPA0	Read data from PA0~PA3 PIN or write data to PA0~PA2 PIN (I/O direction is selected by IOC_PA register)
HRC_ADJ	04H	R/W	0000	X	IADJEN	ADJ1	ADJ0	IADJEN: HRCOSC internal adjust on/off 0: HRCOSC internal adjust disabled 1: HRCOSC internal adjust enabled ADJ1,ADJ0: HRCOSC internal adjust reg.
IOC_PB	05H	R/W	0000	IOCB3	IOCB2	IOCB1	IOCB0	Port PB0~PB3 input/output direction : 1: set port as output port individually 0: set port as input port individually
DATA_PB	06H	R/W	xxxx	DPB3	DPB2	DPB1	DPB0	Read data from PB0~PB3 port or write data to PB0~PB3 (I/O direction is defined by IOC_PB register)
USER1	07H	R/W	xxxx	USER1.3	USER1.2	USER1.1	USER1.0	General purpose user RAM
TMCTL	08H	R/W	0000	TM2EN	TM1EN	TM1SCK	TM1ALD	TM1ALD: Timer 1 auto load control 0 : Timer 1 auto load function turned off 1 : Timer 1 auto load function turned on TM1SCK:Timer1 clock source selection 0: internal clock (frequency selected by SCALER1 register) 1: external clock (from PA2 pin) IOCA2 must be set to 0. TM1EN: Timer 1 enable control bit 0 : Timer 1 disabled 1 : Timer 1 enabled TM2EN: Timer 2 enable control bit 0 : Timer 2 disabled 1 : Timer 2 enabled

ADJ1	ADJ0	Internal HRCOSC frequency
0	0	32MHz + 4%
0	1	32MHz + 2%
1	0	32MHz - 2%
1	1	32MHz - 4%

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SYS0	09H	R/W	0000	TM2MSK	TM1MSK	ENINT	PWMO	**Notice: The PWMO, ENINT, TM1MSK and TM2MSK will be cleared by HALT instruction** PWMO: PWM mode on/off 0 : timer or BZ mode enabled 1 : PWM mode enabled (The frequency of PWM controlled by register TM1BIT and TM1ALD if PWMO=1) ENINT: Global interrupt enable 0 : global interrupt disabled 1 : global interrupt enabled, (ENINT control the interrupt enable of Timer 1, Timer 2 and RTC) TM1MSK : Timer 1 interrupt mask 0 : Timer 1 interrupt mask enabled,Timer1 interrupt disabled. 1 : Timer 1 interrupt mask disabled,Timer1 interrupt enabled. TM2MSK : Timer 2 interrupt mask 0 : Timer 2 interrupt mask enabled.Timer2 interrupt disabled. 1 : Timer 2 interrupt mask disabled,Timer2 interrupt enabled.
TIM1 /PWMD1	0AH	R/W	0000	TIM1.3 (TIM1.7)	TIM1.2 (TIM1.6)	TIM1.1 (TIM1.5) (TIM1.9)	TIM1.0 (TIM1.4) (TIM1.8)	TIM1.9~TIM1.0: 10 bit TIMER 1 counter value, read or write must follow fixed sequence as below. This fixed sequence can be cleared by CLT1T2 register. (1) Write: write **low nibble first**, and then write middle and high nibble. (2) Read: read **low nibble first**, and then read middle and high nibble. PWMD1: If PWM mode is enabled, TIM1 will act as PWMD1 register.
TIM2	0BH	R/W	0000	TIM2.3 (TIM2.7)	TIM2.2 (TIM2.6)	TIM2.1 (TIM2.5)	TIM2.0 (TIM2.4)	TIM2.7~TIM2.0: 8 bit TIMER 2 counter value, read or write must follow fixed sequence as below. This fixed sequence can be cleared by CLT1T2 register. (1) Write: write **low nibble first**, and then write high nibble. (2) Read: read **low nibble first**, and then read high nibble.
IOC_PD	0CH	R/W	0000	IOCD3	IOCD2	IOCD1	IOCD0	Port D input/output direction select 1: set port as output port individually 0: set port as input port individually
DATA_PD	0DH	R/W	xxxx	DPD3	DPD2	DPD1	DPD0	Read port D data from PD0~PD3 port or write data to PD0~PD3 (I/O direction is defined by IOC_PD register)

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<table>
<tr><td>SCALER1</td><td>0EH</td><td>R/W</td><td>0000</td><td>TM1BIT</td><td>T1DIV2</td><td>T1DIV1</td><td>T1DIV0</td><td>T1DIV2~0 : The pre-scaler of Timer 1
Timer 1 clock source definition table:
(FMCK = MCU operating clock)
<table>
<tr><th>T1DIV2</th><th>T1DIV1</th><th>T1DIV0</th><th>TM1CK</th></tr>
<tr><td>0</td><td>0</td><td>0</td><td>FMCK/256</td></tr>
<tr><td>0</td><td>0</td><td>1</td><td>FMCK /128</td></tr>
<tr><td>0</td><td>1</td><td>0</td><td>FMCK /64</td></tr>
<tr><td>0</td><td>1</td><td>1</td><td>FMCK /32</td></tr>
<tr><td>1</td><td>0</td><td>0</td><td>FMCK /16</td></tr>
<tr><td>1</td><td>0</td><td>1</td><td>FMCK /8</td></tr>
<tr><td>1</td><td>1</td><td>0</td><td>FMCK /4</td></tr>
<tr><td>1</td><td>1</td><td>1</td><td>FMCK /2</td></tr>
</table>
TM1BIT: PWM time base resolution selection. (If PWMO is set, the frequency of PWM is controlled by PWM5B, TM1BIT and TM1ALD registers)</td></tr>
<tr><td>USER2</td><td>0FH</td><td>R/W</td><td>xxxx</td><td>USER2.3</td><td>USER2.2</td><td>USER2.1</td><td>USER2.0</td><td>General purpose user RAM</td></tr>
<tr><td>MDCTL</td><td>10H</td><td>W</td><td>1100</td><td>MD1</td><td>MD0</td><td>X</td><td>X</td><td>MCU operation mode selection table
<table>
<tr><th>MD1</th><th>MD0</th><th>MCU MODE</th></tr>
<tr><td>0</td><td>0</td><td>Into HALT mode (or use HALT instruction)</td></tr>
<tr><td>0</td><td>1</td><td>Enters NORMAL mode</td></tr>
<tr><td>1</td><td>0</td><td>Enters GREEN mode</td></tr>
<tr><td>1</td><td>1</td><td>reserved, do not set this value.</td></tr>
</table></td></tr>
<tr><td>ADCCTL</td><td>11H</td><td>R/W</td><td>0000</td><td>TEMPEN</td><td>ADCEN</td><td>ADCST</td><td>EOC
(R)</td><td>EOC: End of A/D conversion
0: A/D conversion in process
1: A/D conversion is completed, the ADCST bit is automatically cleared when EOC rising edge occurred.
ADCST: To start A/D conversion
0: A/D conversion not in progress
1: to start A/D conversion
ADCEN: ADC converter enable control
0: ADC disabled, no operating current.
1: ADC enabled
TEMPEN: Temperature sensor and bandgap enabled control
0: Temperature sensor disabled and bandgap voltage generator enabled
1: Temperature sensor enabled and bandgap voltage generator disabled</td></tr>
<tr><td>CHSEL</td><td>12H</td><td>R/W</td><td>0111</td><td>BRKEN</td><td>ADS2</td><td>ADS1</td><td>ADS0</td><td>BRKEN: PWM brake function enable
0: PWM brake function disabled
1: PWM brake function enabled
ADS2~ADS0: ADC channel selection
<table>
<tr><th>ADS2</th><th>ADS1</th><th>ADS0</th><th>Channel</th></tr>
<tr><td>0</td><td>0</td><td>0</td><td>AN0</td></tr>
<tr><td>0</td><td>0</td><td>1</td><td>AN1</td></tr>
<tr><td>0</td><td>1</td><td>0</td><td>AN2</td></tr>
<tr><td>0</td><td>1</td><td>1</td><td>AN3</td></tr>
<tr><td>1</td><td>0</td><td>0</td><td>AN4</td></tr>
<tr><td>1</td><td>0</td><td>1</td><td>AN5</td></tr>
<tr><td>1</td><td>1</td><td>0</td><td>AN6
(for bandgap or temperature sensor)</td></tr>
<tr><td>1</td><td>1</td><td>1</td><td>All ANn disabled</td></tr>
</table></td></tr>
</table>

ADCCKS	13H	R/W	0000	ADCMSK	ADCFG	ADCK1	ADCK0	ADC clock source selection table ADCK1 | ADCK0 | ADC clock source 0 | 0 | FMCK /2(or FLRCOSC /1) 0 | 1 | FMCK /4(or FLRCOSC /2) 1 | 0 | FMCK /8(or FLRCOSC /4) 1 | 1 | FMCK /16(or FLRCOSC/8) ADCFG: ADC interrupt flag 0: no ADC interrupt occurred 1: ADC interrupt occurred ADCMSK: ADC interrupt mask 0 : ADC interrupt mask enabled, ADC interrupt disabled. 1: ADC interrupt mask disabled, ADC interrupt enabled.
PWMD2	14H	W	xxxx	PWM2.3 (PWM2.7)	PWM2.2 (PWM2.6)	PWM2.1 (PWM2.5) (PWM2.9)	PWM2.0 (PWM2.4) (PWM2.8)	PWM2.9~PWM2.0: 10 bit PWMD2 counter value, read or write must follow fixed sequence as PWMD1. This fixed sequence can be cleared by CLT1T2 register.
PWMD3	15H	W	xxxx	PWM3.3 (PWM3.7)	PWM3.2 (PWM3.6)	PWM3.1 (PWM3.5) (PWM2.9)	PWM3.0 (PWM3.8) (PWM2.8)	PWM3.9~PWM3.0: 10 bit PWMD3 counter value, read or write must follow fixed sequence as PWMD1. This fixed sequence can be cleared by CLT1T2 register.
OVD12	16H	W/R	1111	OVD2H	OVD2L	OVD1H	OVD1L	PWM1 & PWM2 override data
T1CK	17H	R/W	0000	CLT1T2	PWM5B	T1DIV3	PA2BZ	PA2BZ: BZ output by PA2 pin 0: PA2 is normal I/O port 1: If PWMO is cleared, PA2 will act as BZ output T1DIV3: timer1 clock source selection 0: Timer 1 clock source is system clock 1: Timer1 clock source is 32MHz PWM5B: PWM 5 bit mode on/off 0: PWM 5 bit mode disabled 1: PWM 5 bit mode enabled. CLT1T2: Clear all sequence counter of TIM1, TIM2, PWMD2 and PWMD3. 1: clear all sequence counter. 0: no action.
DMA0	18H	R/W	xxxx	DMA0.3	DMA0.2	DMA0.1	DMA0.0	DMA0~DMA2(exclude DMA2.3) build a 11 bit Addressing space for read ROM data. DMA0 is the lowest nibble Address, DMA2 is the highest nibble Address. DMA2.3: It's a user usable register only, it's useless for Address setting.
DMA1	19H	R/W	xxxx	DMA1.3	DMA1.2	DMA1.1	DMA1.0	
DMA2	1AH	R/W	xxxx	DMA2.3	DMA2.2	DMA2.1	DMA2.0	
OVD3	1BH	W/R	XX11	X	X	OVD3H	OVD3L	PWM3 override data
DMDL	1CH	R	xxxx	DMDL.3	DMDL.2	DMDL.1	DMDL.0	DMDL is used to read low nibble data from ROM that Addressed by DMA0 ~ DMA2.
DMDM	1DH	R/W	xxxx	DMDM.3	DMDM.2	DMDM.1	DMDM.0	(1) DMDM is used to read middle nibble data from ROM that Addressed by DMA0 ~ DMA2. (2) Write this register with data 05h will clear watch dog timer (WDT) (3) Write this register with data 0Ah will clear RTC counter.
DMDH	1EH	R	xxxx	DMDH.3	DMDH.2	DMDH.1	DMDH.0	DMDH is used to read high nibble data from ROM that Addressed by DMA0 ~ DMA2.

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SCALER2	1FH	R/W	0000	TM2ALD	T2DIV2	T2DIV1	T2DIV0	T2DIV2~0: The pre-scaler of Timer 2 (F_{MCK} = MCU operating clock)

T2DIV2	T2DIV1	T2DIV0	TM2CK
0	0	0	F_{MCK}/256
0	0	1	F_{MCK} /128
0	1	0	F_{MCK} /64
0	1	1	F_{MCK} /32
1	0	0	F_{MCK} /16
1	0	1	F_{MCK} /8
1	1	0	F_{MCK} /4
1	1	1	F_{MCK} /2

TM2ALD: Timer 2 auto load control
0 : Timer 2 auto load function turned off
1 : Timer 2 auto load function turned on

USER SRAM 256 nibbles	20H~ 3FH	R/W	XXXX	SRAM.3	SRAM.2	SRAM.1	SRAM.0	User SRAM, MAH = 0~7H, use MAH to change SRAM page.

5.5 Extended I/O

TR4P271AT/AF is provided two special instruction “LD **EXIO**(n), A” and LD A, **EXIO**(n), where n = 00H ~ 1FH” to obtain the 32 extra I/O registers. These registers are used for the pull up resistor, wake up, ADC and PWM relative control, they can be accessed by two “LD” data transfer instruction only.

For example, to enable the pull up resistor of port A, the program should be as below:

```
LD A, #FH
LD EXIO(00H), A
```

U: unchanged X: unknown value R/W: readable & writeable R: readable only W: writeable only

Symbol	Addr.	R/W	Reset	D3	D2	D1	D0	Description
PAPU	00H	W	0000	PAPU.3	PAPU.2	PAPU.1	PAPU.0	PA2~PA0 pull up 100K ohm resistor PA3 pull up 60K ohm resistor 0: Port A pull up resistor disabled 1: Port A pull up resistor enabled
PAPL	01H	W	0000	PAPL.3	PAPL.2	PAPL.1	PAPL.0	Port A pull down 100K ohm resistor 0: Port A pull down resistor disabled 1: Port A pull down resistor enabled
PBPU	02H	W	0000	PBPU.3	PBPU.2	PBPU.1	PBPU.0	Port B pull up 100K ohm resistor 0: Port B pull up resistor disabled 1: Port B pull up resistor enabled
PBPL	03H	W	0000	PBPL.3	PBPL.2	PBPL.1	PBPL.0	Port B pull down 100K ohm resistor 0: Port B pull down resistor disabled 1: Port B pull down resistor enabled
PDPU	04H	W	0000	PDPU.3	PDPU.2	PDPU.1	PDPU.0	Port D pull up 100K ohm resistor 0: Port D pull up resistor disabled 1: Port D pull up resistor enabled
PDPL	05H	W	0000	PDPL.3	PDPL.2	PDPL.1	PDPL.0	Port D pull down 100K ohm resistor 0: Port D pull down resistor disabled 1: Port D pull down resistor enabled
PAWK	06H	W	0000	PAWK.3	PAWK.2	PAWK.1	PAWK.0	Port A wake up enable control 0: Port A wake up disabled 1: Port A wake up enabled
PBWK	07H	W	0000	PBWK.3	PBWK.2	PBWK.1	PBWK.0	Port B wake up enable control 0: Port B wake up disabled 1: Port B wake up enabled
PDWK	08H	W	0000	PDWK.3	PDWK.2	PDWK.1	PDWK.0	Port D wake up enable control 0: Port D wake up disabled 1: Port D wake up enabled
ADBH	09H	R	xxxx	AD11	AD10	AD9	AD8	AD11(MSB)~AD0(LSB): 12bit ADC converter result.
ADBM	0AH	R	xxxx	AD7	AD6	AD5	AD4	

ADBL	0BH	R/W	xxxx	AD3	AD2	AD1	AD0	**Note: The clock of ADC would be changed to LRCOSC(458KHz) by writing data 05h to ADBL register. It's would be changed back by writing the others data (except 05h).**
DTIME	0CH	R/W	0000	DTIME3	DTIME2	DTIME1	DTIME0	DTIME2~DTIME0: Dead-time divider DTIME3: Dead time clock source definition. If DTIME3 =0, Dead-time = (DTIME2~0) X Tck Tck = system clock or 32MHz /1, /2, /4, /8 by Dead-time scaler (DTSCAL) If DTIME3 =1, Dead-time = (DTIME2~0) X 3ns
DTSCAL	0DH	R/W	0000	OVSYN	OVSTOP	DTS1	DTS0	DTS1,DTS0: Dead-time pre-scaler selection, reference Table 8 OVSTOP: PWM single shut mode on/off. 0: PWM single shut mode disabled 1: PWM single shut mode enabled OVSYN: override synchronization define 0: override synchronization enabled 1: override synchronization disabled
OVC12	0EH	R/W	0000	OVC2H	OVC2L	OVC1H	OVC1L	Override control register of PWM1/2
OVC3	0FH	R/W	0000	X	X	OVC3H	OVC3L	Override control register of PWM3
RESERVED	**10H~1BH**							reserved
POL12	1CH	R/W	0000	INV2H	INV2L	INV1H	INV1L	PWM1/2 output signal polarity INV1L: PWM1L polarity definition 0: active high (normal mode) 1: active low (reversed mode) INV1H: PWM1L polarity definition INV2L: PWM2L polarity definition INV2H: PWM2H polarity definition Control method same as INV1L
POL3	1DH	R/W	0000	X	X	INV3H	INV3L	INV3L: PWM3L polarity definition 0: active high (normal mode) 1: active low (reversed mode) INV3H: PWM3H polarity definition Control method same as INV3L
PIOEN1	1EH	R/W	0000	P2HEN	P2LEN	P1HEN	P1LEN	P1LEN: PWM1L/PD2 I/O mode control P1HEN: PWM1H/PD1 I/O mode control P2LEN: PWM2L/PD0 I/O mode control P2HEN: PWM2H/PB2 I/O mode control
PIOEN2	1FH	R/W	0000	EINTMSK	EINT_FG	P3HEN	P3LEN	P3LEN: PWM3L/PB1 I/O mode control P3HEN: PWM3H/PB0 I/O mode control EINTFG: External interrupt flag 0: no external interrupt occurred 1: external interrupt occurred EINTMSK: External interrupt mask 0: External interrupt disabled. 1: External interrupt enabled.

5.6 Interrupt Processing

Table 1 **Interrupt vector Address definition**

Event	Vector Address
RESET	00H
System reserved	02H
WAKE UP	04H
System reserved	06H
Timer1(PWM)/Timer2/RTC/ADC/EINT	08H

The interrupt function block diagram is shown below:
When any interrupt request flag (RTCFG, TM1IFG, TM2IFG, EINT_FG or ADCFG) is set to “1”. Interrupt would happen or not. It depends on the interrupt mask (TM1MSK, TM2MSK, EINTMSK or ADCMSK) and global interrupt enable (ENINT) setting. If interrupt mask set to “1” and global interrupt enable set to “1”, Interrupt will be accepted on the next clock after these interrupt request flag set to “1”. The following four procedures are done in one clock cycle by hardware as below:

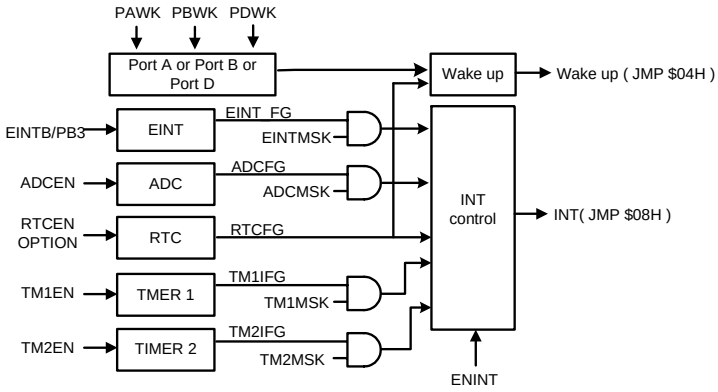

Figure 5 interrupt function block diagram

1. Program Counter, MAH, PCDH and C/Z will be stored in special hardware registers.
2. Program counter will be changed to the corresponding interrupt vector Address.
3. The global interrupt enable register ENINT is automatically stored in special hardware register by hardware circuit.
4. ENINT is cleared to “0”, so interrupt control circuit will be disabled by hardware to avoid unwanted Interrupt event in interrupt handling routine.

When interrupt service routine was finished, an RETI instruction will perform the procedures by hardware as below:

1. Restore the Program Counter, MAH, PCDH and C/Z, which were stored when interrupt happened.
2. The global interrupt enable register ENINT is restore from special register which is automatically stored before interrupt by hardware. This will allow subsequent Interrupt to happen.

The corresponding interrupt request flag must be cleared to “0” by software, before executing RETI instruction. Otherwise, the interrupt procedure will be executed again.
In normal case, if the interrupt accepted by this chip and program jumps into interrupt service routing, the register ENINT must be “1”. It will not accept the interrupt when register ENINT is equal to “0”.
But when clearing ENINT instruction (disable interrupt) is executed, and interrupt happened at next cycle, then the interrupt may still be accepted. This will sometimes causes fault. To avoid this, one "NOP" instruction right after "ENINT clear" is needed.

Notice: Be very careful on the next instruction right after interrupt disabled (ENINT = 0) or timer interrupt mask (TM1MSK=0 or TM2MSK=0). If this instruction contains global variable that is used in both main program and interrupt routine, then it may not work properly(as described above). To ensure the correct operation, one “NOP” instruction right after clearing register ENINT or M1MSK, TM2MSK (set to 0) is needed.

Example: (1) before modified

```
.......
CLR  #1, (SYS0)   ; clear ENINT to zero ( or TM1MSK=0 or TM2MSK=0 )
SET  #1,(XXX)     ; XXX is global variable, interrupt may be accepted at this line and jump to
                  ; interrupt service routing after this instruction (SET #1(xx) ) executed
                  ; successfully. This will be incorrect.
```

(2) after modified

```
.......
CLR  #1, (SYS0)   ; clear ENINT to zero ( or TM1MSK=0 or TM2MSK=0 )
NOP               ; inserted one “NOP” instruction, and ensure next instruction
                  ; SET #1,(XX)  is executed after interrupt disabled ( ENINT=0 )
SET  #1,(XXX)     ; XXX is global variable.
```

5.7 Operation mode

TR4P271AT/AF is provided 3 different modes for low power consumption management by switching around NORMAL mode, GREEN mode and HALT mode.

Commom I/O control register

Symbol	Addr.	R/W	Reset	D3	D2	D1	D0	Description
MDCTL	10H	R/W	1100	MD1	MD0	X	X	MCU operation mode control register

There are three operation modes which are defined at the following table. It can be changed from NORMAL mode to HALT mode or GREEN mode for power saving by setting MD [1:0] of register MDCTL.

MD1	MD0	MCU MODE	HRCOSC or EXTOSC	LRCOSC	MCU clock (F_{MCK})
0	0	into **HALT** mode, or use HALT instruction	stop	enabled	stop
0	1	into **NORMAL** mode **Notice: The "NOP" instruction must be inserted after this command. See Notice 1 as below**	enabled	enabled	(1) HRCOSC------ MCU run 16 MIPS / 8 MIPS /4 MIPS / 1 MIPS by option (2) EXTOSC ----- MCU run at $F_{XTOSC}/2$
1	0	into **GREEN** mode	stop	enabled	MCU run at 114.69KIPS / 57.34KIPS / 28.67KIPS / 14.33KIPS by option
1	1	reserved	-	-	Do not use this value.

Notice 1 : If MCU running in GREEN mode, the following steps will change MCU from GREEN mode to NORMAL mode(MD1,MD0 = 0 1). An additional "NOP" instruction must be inserted right after MDCTL setting instruction.

The state diagram of these three MCU operation modes as below:

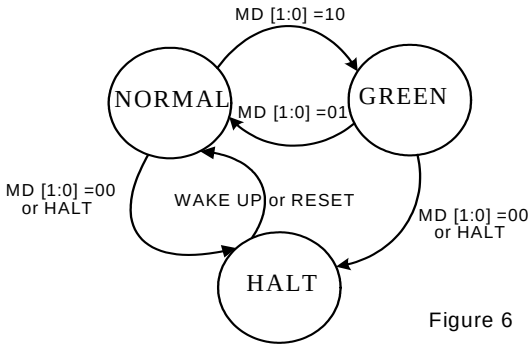

Figure 6

1.NORMAL Mode: In NORMAL mode, both high speed RC oscillator (HRCOSC) and low speed RC oscillator (LRCOSC) are running. MCU clock source is come from HRCOSC oscillator. The default operation mode of TR4P271AT/AF is NORMAL mode after power on. User can change operation mode to HALT mode from NORMAL mode by setting MD [1:0] =00 or execute HALT instruction. If in NORMAL mode, MCU can go to GREEN mode by setting MD[1:0]=10.

2.HALT Mode: In HALT mode, main oscillator HRCOSC is stopped. So the MCU operation is also stopped. But LRCOSC oscillator may still running(if enabled). User can't change the operation mode when in HALT mode. Chip will go back to NORMAL mode when RTC interrupt, I/O wake up or reset occurred. For detail HALT mode description, please refer to section 5.8.

3.GREEN Mode: In GREEN mode, only LRCOSC oscillator keep running, HRCOSC oscillator is stop. MCU uses LRCOSC as system clock source. It's very low speed for low power consumption application. MCU may get to NORMAL mode by setting MD[1:0]=01 if operation speed is not enough. It's also allowed to enter HALT mode by setting MD[1:0]=00 or execute HALT instruction.

5.8 HALT Mode & Wake up

The MCU operation may be switched to HALT mode (MCU operation clock and HRCOSC stop) when HALT instruction executed. It provides a power saving mode for those applications requiring a very low stand-by current. The PA0~PA3, PB0~PB3 and PD0~PD3 are provided with wake up function on rising edge or falling edge. When wake up condition occurred, program will start from $004H Address after stable clock delay (CKstable3 or CKstable4). “system resetb” signal will release HALT state and execute reset procedure. SRAM will keep their previous data without change in HALT mode.

Notice: The register PWMO, ENINT, TMIMSK and TM2MSK will be cleared after wake up by hardware, so re-assign those registers are necessary if interrupt is needed after wake up.

5.9 Watch Dog Timer Reset (WDT)

The watch dog timer (WDT) is used to reset chip when unexpected execution sequence caused, avoiding dead lock of MCU program. This timer can be enabled or disabled by option only. WDT will not have any action when WDT option disabled. Software shall run an "clear watch dog timer" (write data 05h to register $1D) instruction before WDT time out if WDT option is enabled. Hardware will generate a reset signal to reset whole system when WDT overflow. It's provided with four kinds of time-out period (0.125sec~1sec) by WDTS1 and WDTS0 option. The clock source of WDT comes from internal LRCOSC oscillator or external 32k X’tal oscillator. In order to work on HALT mode, these two methods are low power consumption design. If WDT function is enabled by WDT option, the WDT can works in both HALT mode and NORMAL mode, or only works in NORMAL (WDT disabled in HALT mode) by WDTHEN option. If precision clock time is need, the clock source of WDT and RTC will be changed from LRCOSC to 32K X’tal (EXT32K) Oscillator by XT32ENB option enabled, see picture below:

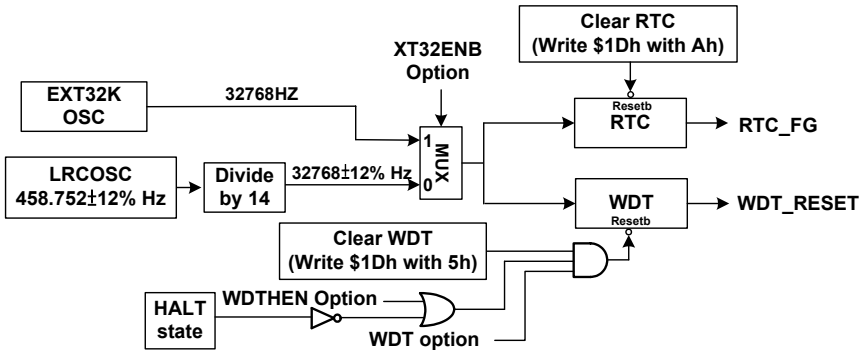

Figure 7. WDT function block diagram

WDT period definition by option

WDTS1	WDTS0	WDT Period
0	0	0.125±12% Sec
0	1	0.25±12% Sec
1	0	0.5±12% Sec
1	1	1.0±12% Sec

Table 2

WDT will be reset when wake up from HALT mode, power on reset, or cleared by software. Reset watch dog timer sequence as below:

```
LD      A, #05H
LD      (1DH), A    ; clear watch dog timer
```

Notice: For good system reliability, It’s strongly recommended that, do not use more than one "reset watch dog" instruction in whole program.

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5.10 Programable 10 bits Timer/Counter--- Timer1

5.10.1 Timer1

The Timer1 is a 10 bit up timer which would be configured as three functions, that is programmable frequency generator (PFD), PWM time base and timer mode. The interrupt interval is generated by selected clock source and specific different values of Timer 1. The content value of Timer 1 is readable or writeable by program.

Timer 1 function definition table

Mode selection	PWMO register	PA2BZ register	PA2 output pin	The six I/O port PD2,PD1,PD0,PB2,PB1 and PB0 act as I/O port or PWM port
Timer mode	0	0	**PA2=DPA2 Register**	**act as I/O port**
PFD mode	0	1	**PA2=BZ signal**	**act as I/O port**
PWM time base mode	1	X	**PA2=DPA2 register**	**act as PWM generator output by setting P[3:1]LEN=111 and P[3:1]HEN=111**

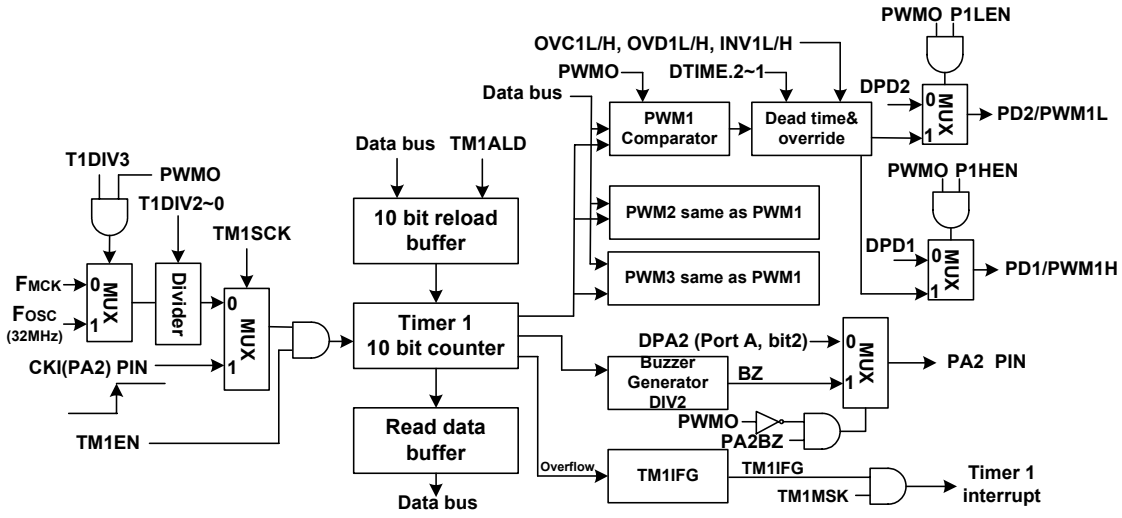

Figure 8 Timer 1 block diagram

Symbol	Addr.	R/W	Reset	D3	D2	D1	D0	Description
STATUS	00H	R/W	00xx	TM2IFG	**TM1IFG**	CF	ZF	TM1IFG: Timer 1 interrupt flag 0: no Timer1 interrupt occurred. 1: Timer1 interrupt occurred, it can be cleared by software.

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TMCTL	08H	R/W	0000	TM2EN	**TM1EN**	**TM1SCK**	**TM1ALD**	TM1ALD: Timer 1 auto load control 0 : Timer 1 auto load function turned off 1 : Timer 1 auto load function turned on TM1SCK:Timer1 clock source selection 0: internal clock (frequency selected by SCALER1 register) 1: external clock (from PA2 pin) IOCA2 must be cleared . TM1EN: Timer 1 enable control bit 0 : Timer 1 disabled 1 : Timer 1 enabled
SYS0	09H	R/W	0000	TM2MSK	**TM1MSK**	**ENINT**	**PWMO**	**Notice: The PWMO, ENINT, TM1MSK and TM2MSK will be cleared by HALT instruction** PWMO: PWM mode on/off 0 : timer or BZ mode enabled 1 : PWM mode enabled (The frequency of PWM controlled by register TM1BIT and TM1ALD if PWMO=1) ENINT: Global interrupt enable 0 : global interrupt disabled 1 : global interrupt enabled, (ENINT control the interrupt enable of Timer 1, Timer 2 and RTC) TM1MSK : Timer 1 interrupt mask 0 : Timer 1 interrupt mask enabled,Timer1 interrupt disabled. 1 : Timer 1 interrupt mask disabled,Timer1 interrupt enabled.
TIM1 /PWMD1	0AH	R/W	0000	**TIM1.3 (TIM1.7)**	**TIM1.2 (TIM1.6)**	**TIM1.1 (TIM1.5) (TIM1.9)**	**TIM1.0 (TIM1.4) (TIM1.8)**	TIM1.9~TIM1.0: 10 bit TIMER 1 counter value, read or write must follow fixed sequence as below. This fixed sequence can be cleared by CLT1T2 register. (1) Write: write **low nibble first**, and then write middle and high nibble. (2) Read: read **low nibble first**, and then read middle and high nibble. PWMD1: If PWM mode is enabled, TIM1 will act as PWMD1 register.
SCALER1	0EH	R/W	0000	**TM1BIT**	**T1DIV2**	**T1DIV1**	**T1DIV0**	TM1BIT: PWM time base resolution selection. (If PWMO is set, the frequency of PWM is controlled by PWM5B, TM1BIT and TM1ALD registers)
T1CK	**17H**	R/W	0000	**CLT1T2**	**PWM5B**	**T1DIV3**	PA2BZ	T1DIV3: timer1 clock source selection 0: Timer 1 clock source is system clock 1: Timer1 clock source is 32MHz PWM5B: PWM 5 bit mode on/off 0: PWM 5 bit mode disabled 1: PWM 5 bit mode enabled. CLT1T2: Clear all sequence counter of TIM1, TIM2, PWMD2 and PWMD3. 1: clear all sequence counter. 0: no action.

The clock source of Timer 1

The clock source of Timer 1 comes from internal clock or external clock CKI (PA2) pin by TM1SCK register. If TM1SCK is set, the event counter would be constructed. The clock source of event counter will come from external CKI pin. It will be counted every rising edge on CKI (PA2) pin.

If TM1SCK is cleared and PWMO is cleared, internal clock source F_{MCK} is selected. There are 8 kinds of clock rate selectable by register T1DIV2~T1DIV0. (see table 3)

Timer 1 clock source table (F_{MCK} = MCU operating clock)

T1DIV2	T1DIV1	T1DIV0	Timer 1 clock in NORMAL Mode (if If F_{MCK} = 16MHz)	Timer 1 clock in GREEN Mode (if If F_{MCK} = 114.69KHz)
0	0	0	F_{MCK} ÷ 256 =62.5KHz	F_{MCK} ÷ 256 = 0.448KHz
0	0	1	F_{MCK} ÷ 128= 125KHz	F_{MCK} ÷ 128 = 0.896KHz
0	1	0	F_{MCK} ÷ 64 = 250KHz	F_{MCK} ÷ 64 = 1.792KHz
0	1	1	F_{MCK} ÷ 32 = 500KHz	F_{MCK} ÷ 32 = 3.584KHz
1	0	0	F_{MCK} ÷ 16 = 1KHz	F_{MCK} ÷ 16 = 7.168KHz
1	0	1	F_{MCK} ÷ 8 = 2MHz	F_{MCK} ÷ 8 = 14.336KHz
1	1	0	F_{MCK} ÷ 4 = 4MHz	F_{MCK} ÷ 4 = 28.672KHz
1	1	1	F_{MCK} ÷ 2 = 8MHz	F_{MCK} ÷ 2 = 57.345KHz

Table 3

Notice: If T1DIV3 is set, Timer1 will not count under GREEN Mode.

Timer 1 interrupts

The Timer1 interrupt interval time and the content value equation is described as follows:
The content value of Timer 1 **= 1024 - (interrupt interval time ÷ Timer 1 clock time period)**
Example: If someone wants to get 360us interrupt interval time, and set T1DIV2~T1DIV0=011, T1DIV3=0, **MCK** = 8MHz. Then Timer 1 clock time period = 1/250k=4us.
so **the content value of Timer 1 = 1024 – (360us/4us) = 934 = 3A6h**

Timer 1 period

The TIM1.9~TIM1.0 content of Timer 1 can be assigned by writing register TIM1 three times. To write this 10 bit value, write low nibble data first, then middle, high nibble data in sequence. To read TIM1 data, read low nibble first then middle, high nibble data in sequence. There is one sequence counter use to handle read or write TIM1 register in sequence. It can be cleared by writing 1 to CLT1T2 register.
The Timer1 counter will be cleared to 000h after TM1EN is cleared or system reset occurred.

Notice 1: The TIM1 register can be assigned data either in interrupt routing or in main program. If in main program, register ENINT must be disabled before write or read data to TIM1. After write or read data to/from TM1 high nibble, ENINT can be enabled if needed.

Notice 2: For good system reliability, It's strongly recommended that, please clear sequence counter by writing 1 to CLT1T2 register before writing three nibbles data to TIM1 register.

Example : in main program

```
.......
CLR   #1, (SYS0)   ; ENINT=0, ENINT disabled
NOP                ; added NOP instruction
LD    A,(T1CK)
OR    A,#08H
LD    (T1CK),A     ; write 1 to CLT1T2 register to clear sequence counter before writing data to TIM1
LD     A,#DH       ; setting TIM1 low nibble first
LD     (TIM1),A
LD     A,#FH       ; setting TIM1 middle nibble
LD     (TIM1),A
LD     A,#0H       ; setting TIM1 high nibble
LD     (TIM1),A
SET   #1,(SYS0)    ; ENINT=1,  ENINT enabled
.......
```

The auto load function is enabled by setting TM1ALD to 1, This 10 bits data will be reloaded into 10 bits up counter while Timer 1 overflow occurred. The interrupt mask control register (TM1MSK) of Timer 1 is used to inhibit interrupt request for MCU. TM1MSK value will not affect normal Timer 1 operation. Even when TM1MSK is masked, TM1IFG will still be set to 1 when overflow, and Timer 1 still keep running. The global interrupt control register (ENINT) should be set to 1 before Timer 1 start. After setting of these control registers, software can enable Timer 1 counter with register TM1EN set to 1. Then Timer 1 will issue an interrupt request (register TM1IFG=1) when the Timer 1 counts from **3FFH to 000H.**

5.10.2 Three channel PWM Generators (use Timer 1 as time base)

The Timer1 could act as PWM Time Base (PTB) by setting PWMO to 1, named PWM mode. In this mode, It is provided three channel PWM generators and each channel has a pair of complementary PWM outputs or independent PWM output. The three PWM generators provide fixed frequency PWM output with 10 bit resolution. The block diagram of PWM is shown in Figure 8.

PWM Time Base

All three PWM generators use same PWM Time Base (PTB) that configured from Timer1. In PWM mode, PTB provides 5~10 bits resolution by register setting register PWM5B, TM1ALD and TM1BIT as shown in see table 4.

Clock source of PWM Time Base

The clock source of PTB comes from internal clock or external clock CKI(PA2) pin by TM1SCK register.
If TM1SCK is set, the PTB clock source comes from external CKI pin.
If TM1SCK is cleared, there are two kinds of clock source selected by T1DIV3 register.
(a) IF T1DIV3 is set, The PTB clock source comes from Fosc (32MHz).
(b) IF T1DIV3 is cleared, the PTB clock source comes from the divided frequency from F_{MCK}. There are eight kinds of clock rate selectable by register T1DIV2~T1DIV0 to PTB. (see table 3)
In PWM mode, the PTB counter will be cleared to 000h after TM1EN set to 1.

Maximum and minimum PWM frequencies

The PWM gives frequency output range from 500KHz (5 bits resolution) to 3.814Hz (10 bit resolution) by setting T1DIV2~T1DIV0, PWM5B, TM1ALD and TM1BIT registers.

In NORMAL Mode, if PWMO is set to 1 and using F_{MCK} as PWM clock source by clearing T1DIV3 to 0. The max. and min. PWM frequency is as in Table 4 below:

PWM5B	TM1ALD	TM1BIT	Res.	Timer 1 value	Max. PWM frequency Set F_{MCK} = 16MHz T1DIV2~0=111	Min. PWM frequency Set F_{MCK} = 1MHz T1DIV2~0=000
0	0	0	10bit	000h~3FFh	(F_{MCK} ÷ 2) ÷ 1024 = 7.8125K	(F_{MCK} ÷ 256) ÷1024 = 3.814Hz
0	0	1	8bit	000h~0FFh	(F_{MCK} ÷ 2) ÷ 256 = 31.25K	(F_{MCK} ÷ 256) ÷ 256 = 24.4Hz
0	1	0	7bit	000h~07Fh	(F_{MCK} ÷ 2) ÷ 128 = 62.5K	(F_{MCK} ÷ 256) ÷ 128 = 30.5Hz
0	1	1	6bit	000h~03Fh	(F_{MCK}÷ 2) ÷ 64 = 125K	(F_{MCK} ÷ 256) ÷ 64 = 61Hz
1	X	X	5bit	000H~01Fh	(F_{MCK}÷ 2) ÷ 32 = 250K	(F_{MCK} ÷ 256) ÷ 32 = 122Hz

Table 4

In NORMAL Mode, if PWMO is set to 1 and use 32MHz as PWM clock source by setting T1DIV3 to high. The max. and min. PWM frequency is as in Table 5 below:

PWM5B	TM1ALD	TM1BIT	Res.	Timer 1 value	Max. PWM frequency PWM clock source is 32MHz, T1DIV2~0=111	Min. PWM frequency PWM clock source is 32MHz, T1DIV2~0=000
0	0	0	10bit	000h~3FFh	(32MHz ÷ 2)÷1024= 15.625K	(32MHz ÷ 256) ÷ 1024 = 122Hz
0	0	1	8bit	000h~0FFh	(32MHz ÷ 2) ÷ 256 = 62.5K	(32MHz ÷ 256) ÷ 256 = 488Hz
0	1	0	7bit	000h~07Fh	(32MHz ÷ 2) ÷ 128 = 125K	(32MHz ÷ 256) ÷ 128 = 976Hz
0	1	1	6bit	000h~03Fh	(32MHz÷ 2) ÷ 64 = 250K	(32MHz ÷ 256) ÷ 64 = 1953Hz
1	X	X	5bit	000H~01Fh	(32MHz÷ 2) ÷ 32 = 500K	(32MHz ÷ 256) ÷ 32 = 3906Hz

Table 5

PWM duty cycle

The duty cycle of PWM1, PWM2 and, PWM3 are defined by PWMD1, PWMD2 and PWMD3 registers. Each register is write only register which stores 10 bit values by writing three times data in same register, writing these registers must follow low nibble first and middle, high nibble in sequence. The PWMD1, PWMD2 and

PWMD3 registers are a double-buffered register, and the content are reloaded into real register when PTB overflow occurred. The overflow is occurred when PTB counter value from 000h to 001h.

Symbol	Addr.	R/W	Reset	D3	D2	D1	D0	Description
TIM1 /PWMD1	0AH	R/W	0000	**TIM1.3 (TIM1.7)**	**TIM1.2 (TIM1.6)**	**TIM1.1 (TIM1.5) (TIM1.9)**	**TIM1.0 (TIM1.4) (TIM1.8)**	TIM1.9~TIM1.0: 10 bit TIMER 1 counter value, read or write must follow fixed sequence as below. This fixed sequence can be cleared by CLT1T2 register. (1) Write: write **low nibble first**, and then write middle and high nibble. (2) Read: read **low nibble first**, and then read middle and high nibble. PWMD1: If PWM mode is enabled, TIM1 will act as PWMD1 register.
PWMD2	**14H**	**W**	**xxxx**	**PWM2.3 (PWM2.7)**	**PWM2.2 (PWM2.6)**	**PWM2.1 (PWM2.5) (PWM2.9)**	**PWM2.0 (PWM2.4) (PWM2.8)**	PWM2.9~PWM2.0: 10 bit PWMD2 counter value, read or write must follow fixed sequence as PWMD1. This fixed sequence can be cleared by CLT1T2 register.
PWMD3	**15H**	**W**	**xxxx**	**PWM3.3 (PWM3.7)**	**PWM3.2 (PWM3.6)**	**PWM3.1 (PWM3.5) (PWM2.9)**	**PWM3.0 (PWM3.8) (PWM2.8)**	PWM3.9~PWM3.0: 10 bit PWMD3 counter value, read or write must follow fixed sequence as PWMD1. This fixed sequence can be cleared by CLT1T2 register.

PWM Time Base interrupts

In PWM mode, an interrupt request is generated every overflow occurred. The detail timing waveform about PTB and interrupt request is as shown below:

Example: PWM1H output waveform (PWM5B=0, TM1ALD=1, TM1BIT=1)

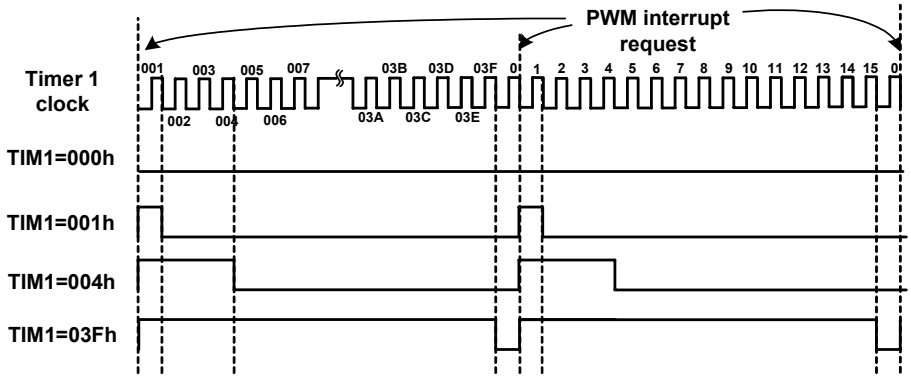

Figure 9. PWM timing waveform

PWM Single Shut mode

The PTB supports single shut mode by OVSTOP register set to 1. PWM could output one pulse by setting TM1EN to high. The TM1EN register will be automatically cleared to low when PWM overflow occurred. In this mode, interrupt request is still work.

Extend I/O

Symbol	Addr.	R/W	Reset	D3	D2	D1	D0	Description
DTSCAL	0DH	R/W	0000	OVSYN	**OVSTOP**	DTS1	DTS0	OVSTOP: PWM single shut mode on/off. 0: PWM single shut mode disabled 1: PWM single shut mode enabled

PWM output share pin configuration

The three channel PWM has six PWM pins which shared with General Purpose I/O (GPIO) by register PIOEN1 and PIOEN2. The GPIO mentioned above are PD0~PD2 and PB0~PB2. The complimentary PWM outputs can be either a single output PWM1L (or PWM1H) or a complimentary pair of outputs PWM1L and PWM1H. To do this flexibility selection is as shown in Table 6 below. IF P1LEN register is set to 1, the PD2 pin acts as PWM1L pin for PWM signal output. Otherwise, P1HEN register is cleared, the PD2 pin acts as a PD2 GPIO function.

I/O function configuration table (register PWMO must be set to 1 first)

I/O Port shared pin	PWM function	GPIO function
PD2/ PWM1L	PD2 acts as PWM1L (set P1LEN = 1)	PD2 acts as PD2 GPIO (set P1LEN = 0)
PD1/ PWM1H	PD1 acts as PWM1H (set P1HEN = 1)	PD1 acts as PD1 GPIO (set P1HEN = 0)
PD0/ PWM2L	PD0 acts as PWM2L (set P2LEN = 1)	PD0 acts as PD0 GPIO (set P2LEN = 0)
PB2/ PWM2H	PB2 acts as PWM2H (set P2HEN = 1)	PB2 acts as PB2 GPIO (set P2HEN = 0)
PB1/ PWM3L	PB1 acts as PWM3L (set P3LEN = 1)	PB1 acts as PB1 GPIO (set P3LEN = 0)
PB0/ PWM3H	PB0 acts as PWM3H (set P3HEN = 1)	PB0 acts as PB0 GPIO (set P3HEN = 0)

Table 6

Extend I/O

Symbol	Addr.	R/W	Reset	D3	D2	D1	D0	Description
PIOEN1	1EH	R/W	0000	**P2HEN**	**P2LEN**	**P1HEN**	**P1LEN**	P1LEN: PWM1L/PD2 I/O mode control P1HEN: PWM1H/PD1 I/O mode control P2LEN: PWM2L/PD0 I/O mode control P2HEN: PWM2H/PB2 I/O mode control
PIOEN2	1FH	R/W	0000	EINTMSK	EINT_FG	**P3HEN**	**P3LEN**	P3LEN: PWM3L/PB1 I/O mode control P3HEN: PWM3H/PB0 I/O mode control

PWM output override

PWM output signal may be manually overridden by specified appropriate data in OVC12, OVC3, OVD12 and OVD3 registers. The OVC12 and OVC3 determine which PWM pins will be overridden. They are all active high.

When the OVC1L~OVC3L or OVC1H~OVC3H bits are set. The logic state of corresponding pins will be controlled by OVD1L~OVD3L or OVD1H~OVD3H. In other words, the register OVD12 and OVD3 determine the logic state of the PWM pins if overridden mode is available.

When the OVC1L~OVC3L and OVC1H~OVC3H bits are cleared, the PWM signal will pass on the corresponding PWM pin

Please see example and block diagram as follows.

For example: (The P1LEN and PWMO bits are set first)

(1) If OVC1L bit is set (override available), the state of PD2 pin is depend on OVD1L bit (PD2 acts as OVD1L).

(2) If OVC1L bit is cleared, the PWM1 signal state will pass to PD2 pin.

All the complementary PWM pins support override mode with Dead-time control. Refer to block diagram as shown below. If the P1LEN, PWMO, P1HEN and OVC1L bits are set, OVC1H and INV1H are cleared, OVD1H and INV1L has no effect, PWM1L and PWM1H pin will be the complementary PWM output of OVD1L with Dead-time control.

Common I/O

Symbol	Addr.	R/W	Reset	D3	D2	D1	D0	Description
OVD12	**16H**	**W/R**	**1111**	**OVD2H**	**OVD2L**	**OVD1H**	**OVD1L**	PWM1 & PWM2 override data
OVD3	**1BH**	**W/R**	**XX11**	X	X	**OVD3H**	**OVD3L**	PWM3 override data

Extend I/O

Symbol	Addr.	R/W	Reset	D3	D2	D1	D0	Description
OVC12	0EH	R/W	0000	**OVC2H**	**OVC2L**	**OVC1H**	**OVC1L**	Override control register of PWM1/2
OVC3	0FH	R/W	0000	X	X	**OVC3H**	**OVC3L**	Override control register of PWM3

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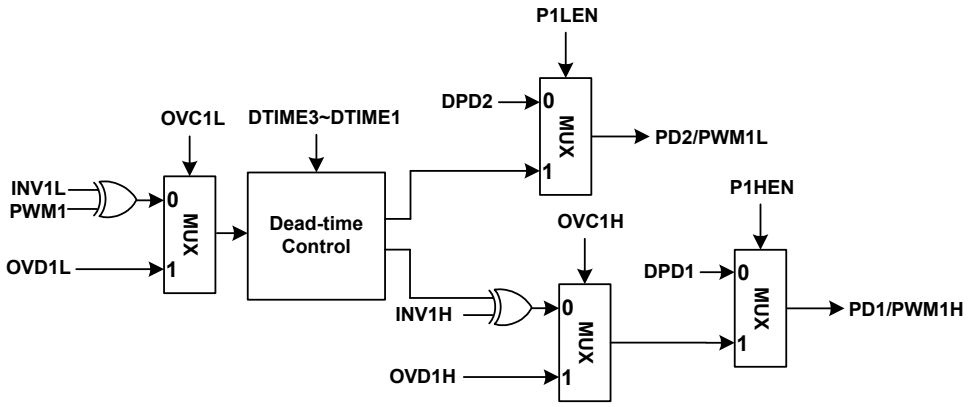

Figure 10. PWM output structure

Override synchronization

If the OVSYN bit of the DTSCAL register is set, all output overrides performed via the OVC12, OVC3, OVD12 and OVD3 bits will be synchronized to the PTB. Synchronous output overrides will occur on the overflow of PTB.

Symbol	Addr.	R/W	Reset	D3	D2	D1	D0	Description
DTSCAL	0DH	R/W	0000	**OVSYN**	OVSTOP	DTS1	DTS0	OVSYN: override synchronization define 0: override synchronization enabled 1: override synchronization disabled

PWM Dead-time generator

If PWMs are used to control the upper and lower switches of a H-bridge, a Dead-time insertion is highly recommended. This avoids any overlap in the switching during the state change of power MOS in the H-bridge device. The Dead-time insertion waveform is as shown below Figure 11.

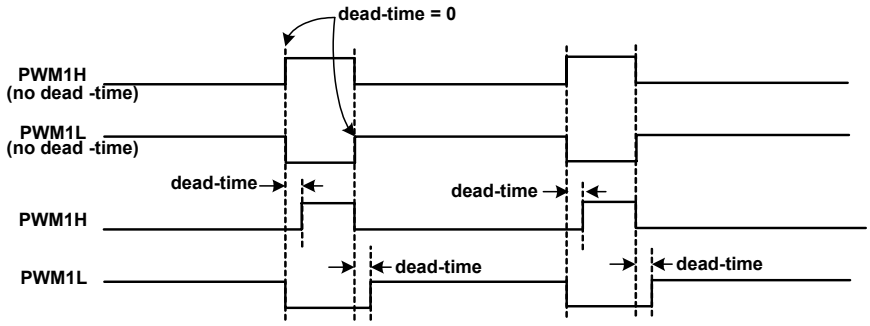

Figure 11. PWM Dead-time waveform

Extend I/O

Symbol	Addr.	R/W	Reset	D3	D2	D1	D0	Description
DTIME	0CH	R/W	0000	**DTIME3**	**DTIME2**	**DTIME1**	**DTIME0**	DTIME2~DTIME0: Dead-time divider DTIME3: Dead time clock source definition. If DTIME3 =0, Dead-time = (DTIME2~0) X Tck Tck = system clock or 32MHz /1, /2, /4, /8 by dead-time scaler (DTSCAL) If DTIME3 =1, dead-time = (DTIME2~0) X 3ns

DTSCAL	0DH	R/W	0000	OVSYN	OVSTOP	**DTS1**	**DTS0**	DTS1,DTS0: Dead-time pre-scaler selection, reference Table 8 OVSTOP: PWM single shut mode on/off. 0: PWM single shut mode disabled 1: PWM single shut mode enabled OVSYN: override synchronization define 0: override synchronization enabled 1: override synchronization disabled
T1CK	**17H**	R/W	0000	CLT1T2	PWM5B	**T1DIV3**	PA2BZ	T1DIV3: timer1 clock source selection 0: Timer 1 clock source is system clock 1: Timer1 clock source is 32MHz

The Dead-time generator provides 3 modes Dead-time by register T1DIV3 and DTIME3.
If T1DIV3 and DTIME3 are cleared, Mode 1 Dead-time is selected. In this mode, Dead-time can be generated from (1/FMCK) – Td to 14/ FMCK by setting register DTIME2 ~ DTIME0, DTS1 and DTS0.
If T1DIV3 is cleared and DTIME3 is set, Mode 2 Dead-time is selected. In this mode, Dead-time can be changed from 1ns to 27ns. Due to apply delay cell scheme in this mode, the Dead-time has some different between every chip.
If T1DIV3 and DTIME3 are cleared, Mode 3 Dead-time is selected. In this mode, the Dead-time clock source comes from 32MHz. The range of Dead-time can be generated from 31.25ns -Td to 437.5ns by setting register DTIME2 ~ DTIME0, DTS1 and DTS0.

Dead-time definition table is as shown below:

Dead-time definition table (Td1=30ns, Td2=12ns)

Reg. Type	T1DIV3	DTIME3	DTIME2	DTIME1	DTIME0	Dead-time (Notice 2) DTS1,DTS0 = 0 1	DTS1,DTS0 = 0 0
Mode1 (Set clock Source from FMCK)	0	0	0	0	0	0ns ~8ns	
		0	0	0	1	(2/ FMCK) x 1	((1/ FMCK) x1) – Td1
		0	0	1	0	(2/ FMCK) x 2	((1/ FMCK) x2) – Td1
		0	0	1	1	(2/ FMCK) x 3	((1/ FMCK) x3) – Td1
		0	1	0	0	(2/ FMCK) x 4	((1/ FMCK) x4) – Td1
		0	1	0	1	(2/ FMCK) x 5	((1/ FMCK) x5) – Td1
		0	1	1	0	(2/ FMCK) x 6	((1/ FMCK) x6) – Td1
		0	1	1	1	(2/ FMCK) x 7	((1/ FMCK) x7) – Td1
Mode 2 (Set clock Source from delay cell)	0	1	0	0	0	* 1ns ~ 4 ns	
		1	0	0	1	* 5ns ~ 8 ns	
		1	0	1	0	* 7ns ~ 11 ns	
		1	0	1	1	* 9ns ~ 13 ns	
		1	1	0	0	* 12ns ~16 ns	
		1	1	0	1	* 6ns ~ 20 ns	
		1	1	1	0	* 20ns ~ 24 ns	
		1	1	1	1	* 22ns ~ 27ns	
Mode 3 (Set clock Source from 32MHz)	1	0	0	0	0	2ns ~ 5ns	
			0	0	1	62.5ns (2/32MHz)	31.25ns – Td2
			0	1	0	125ns (4/32MHz)	62.50ns – Td2
			0	1	1	187.5ns (6/32MHz)	93.75ns – Td2
			1	0	0	250ns (8/32MHz)	125.00ns - Td2
			1	0	1	312.5ns(10/32MHz)	156.25ns - Td2
			1	1	0	375ns (12/32MHz)	187.50ns - Td2
			1	1	1	437.5 (14/32MHz)	218.75ns - Td2

Notice 1: For mass production chips, there is some different in every chips. The dead-time with the asterisk "*" mark,Td1 and Td2 is typical value for reference.

Table 7

The Dead-time clock source comes from 32MHz or system clock FMCK by T1DIV3 bit. These two clock sources can be pre-divided by 2 or 1 using register DTS1 and DTS0.
Dead-time clock period definition is as shown below:

Dead-time clock period (Tck) definition

DTS1	DTS0	TIDIV3=1	TIDIV3=0
0	0	Tck = 1 ÷ 32MHz	Tck = 1 ÷ FMCK
0	1	Tck = 2 ÷ 32MHz	Tck = 2 ÷ FMCK
1	X	Don't use	

Table 8

If register TIDIV3 and DTIME3 are cleared, the range of the maximum and minimum dead-time value are as shown below: (Td = 30ns ,Vdd=3.3v)

MIPS	Pre-scaler selection (Tck)	Min. dead-time (Tck)	Max. dead-time (Tckx7)
16	DTS1 DTS0=00 , 1 ÷ FMCK	1 ÷ 16MHz = 62.5ns-Td	0.437us-Td
16	DTS1 DTS0=01 , 2 ÷ FMCK	2 ÷ 16MHz = 125ns	0.875us
8	DTS1 DTS0=00 , 1 ÷ FMCK	1 ÷ 8MHz = 125ns -Td	0.875us-Td
8	DTS1 DTS0=01 , 2 ÷ FMCK	2 ÷ 8MHz = 250ns	1.75us
4	DTS1 DTS0=00 , 1 ÷ FMCK	1 ÷ 4MHz = 250ns -Td	1.75us-Td
4	DTS1 DTS0=01 , 2 ÷ FMCK	2 ÷ 4MHz = 500ns	3.5us
1	DTS1 DTS0=00 , 1 ÷ FMCK	1 ÷ 1MHz = 1us-Td	7us-Td
1	DTS1 DTS0=01 , 2 ÷ FMCK	2 ÷ 1MHz = 2us	14us

Table 9

If TIDIV3 register is set, the range of the dead-time value is as shown below:

MIPS	Pre-scaler selection (Tck)	Min. dead-time (Tck)	Max. dead-time (Tckx7)
1~16	DTS1 DTS0=00 , 1 ÷ 32MHz	1 ÷ 32MHz = 31.25ns - Td	218.75ns - Td
	DTS1 DTS0=01 , 2÷ 32MHz	2 ÷ 32MHz = 62.5ns	437.5ns

Table 10

PWM output polarity control

The polarity of PWM1L~PWM3L, PWM1H~PWM3H pins can be set 1 or 0 by INV3L~INV1L or INV3H ~ INV3H corresponding bits. If the polarity of PWM1L needs to be inversed, the corresponding control bit INV1L of POL12 register must be set to 1.

Extend I/O

Symbol	Addr.	R/W	Reset	D3	D2	D1	D0	Description
POL12	1CH	R/W	0000	**INV2H**	**INV2L**	**INV1H**	**INV1L**	PWM1/2 output signal polarity INV1L: PWM1L polarity definition 0: active high (normal mode) 1: active low (reversed mode) INV1H: PWM1L polarity definition INV2L: PWM2L polarity definition INV2H: PWM2H polarity definition Control method same as INV1L
POL3	1DH	R/W	0000	X	X	**INV3H**	**INV3L**	INV3L: PWM3L polarity definition 0: active high (normal mode) 1: active low (reversed mode) INV3H: PWM3H polarity definition Control method same as INV3L

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PWM brake input (EINTB/PB3)

Common I/O

Symbol	Addr.	R/W	Reset	D3	D2	D1	D0	Description
CHSEL	12H	R/W	0111	**BRKEN**	ADS2	ADS1	ADS0	BRKEN: PWM brake function enabled/ disabled 0: PWM brake function disabled 1: PWM brake function enabled

Extend I/O

Symbol	Addr.	R/W	Reset	D3	D2	D1	D0	Description
PIOEN2	1FH	R/W	0000	**EINTMSK**	**EINT_FG**	P3HEN	P3LEN	EINTFG: External interrupt flag 0: no external interrupt occurred 1: external interrupt occurred EINTMSK: External interrupt mask 0: External interrupt disabled. 1: External interrupt enabled.

When PWM is running, the PWM function can be disabled by external brake pin BRAKE/PB3 immediately. All PWM output pins will be changed to an inactive state. In order to response quickly for any accident condition, the brake function is performed directly by hardware after brake pin BRAKE/PB3 falling edge occurred.

The brake function is enabled by setting BRKEN bit to 1. The brake pin BRAKE/PB3 is falling edge triggered, so it is easy to wire-or many trigger sources to BRAKE/PB3 pin. The EINT_FG bit is a common bit for brake function and external interrupt flag, it will be set if BRAKE/PB3 falling edge occurred. If brake function is enabled and BBRAKE/PB3 falling edge occurred, TR4P271AT/AF will set PWM outputs into an inactive state immediately. In this condition, it can save the power devices which connected to the PWM pins. The brake function and external interrupt block diagram is as shown below:

Notice: Please clear EINT_FG bit before BRKEN set to 1.

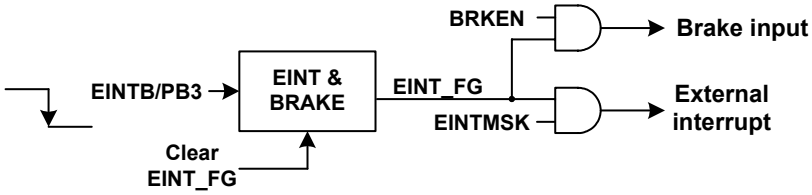

Figure 12. Brake & external interrupt block diagram

External interrupt

TR4P271AT/AF provides one external interrupt EINTB/PB3 pin. The interrupt flag EINT_FG is used to indicate external interrupt occurred. It also provides interrupt mask bit EINTMSK to inhibit external interrupt function.

Notice: Please clear EINT_FG bit before EINTMSKL set to 1.

5.10.3 Programmable Frequency Divider (PFD)---- (use Timer 1)

Timer 1 could be configured as programmable frequency divider (PFD) by setting PA2BZ to 1 and PWMO to 0, can output single tone signal to BZ (PA2) pin. No interrupt will occur in this mode. If F_{MCK} is 8 MIPS, the frequency of PFD ranges from 61Hz to 2MHz in NORMAL mode, duty cycle 50%, with square wave output. It's suitable for driving buzzer or other applications. Timer 1 can be regarded as a programmable frequency divider. Its frequency is selected by register T1DIV2~T1DIV0 and combining the operation of content value of Timer 1.

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Symbol	Addr.	R/W	Reset	D3	D2	D1	D0	Description
T1CK	17H	R/W	0000	CLT1T2	PWM5B	T1DIV3	PA2BZ	PA2BZ: BZ output by PA2 pin 0: PA2 is normal I/O port 1: If PWMO is cleared, PA2 will act as BZ output

The clock source of PFD generator comes from MCU clock (F_{MCK}) that depends on current MCU operation and oscillator mode. So MCU clock (F_{MCK}) may be HRCOSC (16 MIPS, 8 MIPS, 4 MIPS, 1 MIPS), LRCOSC (114.69KIPS, 57.34KIPS, 28.67KIPS, 14.33KIPS) or EXTOSC (16 MIPS~0.5 MIPS)

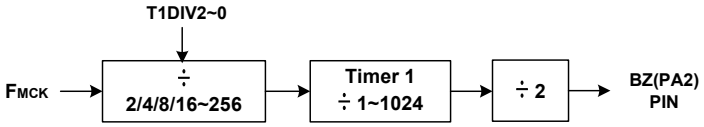


Figure 13.PFD clock diagram

If F_{MCK} is 16MHz, in NORMAL Mode, the BZ (PA2) clock output is as shown below:

T1DIV2	T1DIV1	T1DIV0	BZ(PA2) clock output
0	0	0	(F_{MCK} ÷ 256) ÷ (1~1024) ÷ 2 = 30.52Hz ~ 31.25KHz
0	0	1	(F_{MCK} ÷ 128) ÷ (1~1024) ÷ 2 = 61.03Hz ~ 62.5KHz
0	1	0	(F_{MCK} ÷ 64) ÷ (1~1024) ÷ 2 = 122.07Hz ~ 125KHz
0	1	1	(F_{MCK} ÷ 32) ÷ (1~1024) ÷ 2 = 244.14Hz ~ 250KHz
1	0	0	(F_{MCK} ÷ 16) ÷ (1~1024) ÷ 2 = 488.28Hz ~ 500KHz
1	0	1	(F_{MCK} ÷ 8) ÷ (1~1024) ÷ 2 = 976.56Hz ~ 1000KHz
1	1	0	(F_{MCK} ÷ 4) ÷ (1~1024) ÷ 2 = 1.953Hz ~ 2000KHz
1	1	1	(F_{MCK} ÷ 2) ÷ (1~1024) ÷ 2 = 3.906KHz ~ 4000KHz

Table 11

5.11 Programable 8 bits Timer2

The Timer 2 is an 8 bit up timer. The interrupt interval is determined by selected clock source and written data of Timer 2. The content of Timer 2 can be read or write by software.

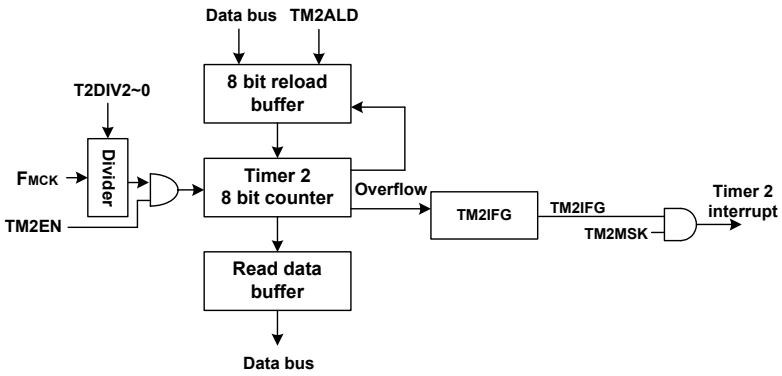


Figure 14. Timer 2 block diagram

Symbol	Addr.	R/W	Reset	D3	D2	D1	D0	Description
STATUS	00H	R/W	00xx	**TM2IFG**	TM1IFG	CF	ZF	TM2IFG: Timer 2 interrupt flag 0: no Timer 2 interrupt occurred. 1: Timer2 interrupt occurred, it can be cleared by software.
SYS0	09H	R/W	0000	**TM2MSK**	TM1MSK	**ENINT**	PWMO	**Notice: The PWMO, ENINT, TM1MSK and TM2MSK will be cleared by HALT instruction** ENINT: Global interrupt enable 0 : global interrupt disabled 1 : global interrupt enabled, (ENINT control the interrupt enable of Timer 1, Timer 2 and RTC) TM2MSK : Timer 2 interrupt mask 0 : Timer 2 interrupt mask enabled.Timer2 interrupt disabled. 1 : Timer 2 interrupt mask disabled,Timer2 interrupt enabled.
TIM2	0BH	R/W	0000	**TIM2.3 (TIM2.7)**	**TIM2.2 (TIM2.6)**	**TIM2.1 (TIM2.5)**	**TIM2.0 (TIM2.4)**	TIM2.7~TIM2.0: 8 bit TIMER 2 counter value, read or write must follow fixed sequence as below. This fixed sequence can be cleared by CLT1T2 register. (1) Write: write **low nibble first**, and then write high nibble. (2) Read: read **low nibble first**, and then read high nibble.
SCALER2	1FH	R/W	0000	**TM2ALD**	**T2DIV2**	**T2DIV1**	**T2DIV0**	T2DIV2~0: The pre-scaler of Timer 2 (F_{MCK} = MCU operating clock) TM2ALD: Timer 2 auto load control 0 : Timer 2 auto load function turned off 1 : Timer 2 auto load function turned on

The clock source of Timer 2 is internal clock. There are 8 kinds of clock rate setting by register T1DIV2~T1DIV0.

Table 12, TM2CK= Timer 2 clock source (F_{MCK} = MCU operating clock)

T2DIV2	T2DIV1	T2DIV0	TM2CK
0	0	0	F_{MCK} /256
0	0	1	F_{MCK} /128
0	1	0	F_{MCK} /64
0	1	1	F_{MCK} /32
1	0	0	F_{MCK} /16
1	0	1	F_{MCK} /8
1	1	0	F_{MCK} /4
1	1	1	F_{MCK} /2

The 8 bits content of Timer 2 can be assigned by register TIM2.7~TIM2.0. To write this 8 bit value, write low nibble first and then high nibble. To read TIM2.7~TIM2.0, read low nibble first then read high nibble. When TM2ALD is set to 1, this 8 bits data will be reloaded into 8 bits up counter when overflow occurs.

The interrupt mask control register (TM2MSK) of Timer 2 is used to inhibit interrupt request for MCU. TM2MSK value will not affect normal Timer 2 operation. Even when TM2MSK is masked, TM1IFG will still be set to 1 when timer overflow occurred, and Timer 2 still keep running. The global interrupt control register (ENINT) should be set to 1 before Timer 2 start. After setting of these control registers, software can enable Timer 2 counter with register TM2EN set to 1. Then Timer 2 will issue an interrupt request (register TM2IFG=1) when the Timer 2 counts from FFH to 00H.

Notice 1: The TIM2 registers must be read or written twice (low nibble first and high nibble later) in sequence. Only one nibble read or write is prohibited.

Notice 2: The TIM2 register can be assigned data either in interrupt routing or in main program. If in main program, register ENINT must be disabled before write or read data to TIM2. After write or read data to/from TM2 high nibble, ENINT can be enabled if needed.

Example : in main program

…….

```
CLR   #1, (SYS0)   ; ENINT=0 ENINT disabled
NOP                ; added NOP instruction
LD    A,#DH        ; setting TIM2 low nibble first
LD    (TIM2),A
LD    A,#FH        ; setting TIM2 high nibble later
LD    (TIM2),A
SET   #1,(SYS0)    ; ENINT=1 ENINT enabled
```

5.12 Real time clock interrupt (RTC)

Symbol	Addr.	R/W	Reset	D3	D2	D1	D0	Description
RTC	01H	R/W	0000	**RTCFG**	F38K	**RTCS1**	**RTCS0**	RTC will cause an interrupt ($008h) when in NORMAL mode or GREEN mode. In HALT mode, RTC can wake up MCU and program will go to wake up vector ($004h). RTCS1, RTCS0: RTC interrupt period detailed description in Real Time Clock Interrupt section. RTCFG: RTC overflow flag 0: RTC overflow not occurred. 1: RTC overflow occurred, it can be cleared by software.
DMDM	1DH	R/W	xxxx	DMDM.3	DMDM.2	DMDM.1	DMDM.0	Write this register with data 0Ah will clear RTC counter.

RTC function is enabled by RTCEN option. If RTCEN option is enabled, It will keep running at NORMAL and HALT mode. There are two different interrupt jump Address supported after RTC overflow occurred.
If MCU operates in NORMAL/GREEN mode, it will jump to Address $008 after RTC overflow occurred. If MCU is in HALT mode, RTC overflow will wake-up chip and jump to Address $004. The RTCFG flag is set every 0.125sec~1sec (or 15.625ms ~ 125ms, by setting register RTCS1, RTCS0 and SPUP option) as below:

RTCS1, RTCS0: RTC interrupt period selection

RTCS1	RTCS0	RTC Period	
		SPUP option enabled	**SPUP option disabled**
0	**0**	0.125±12% Sec	15.625±12% ms
0	**1**	0.25±12% Sec	31.25±12% ms
1	**0**	0.5 ±12% Sec	62.5 ±12% ms
1	**1**	1.0 ±12% Sec	125 ±12% ms

Table 13

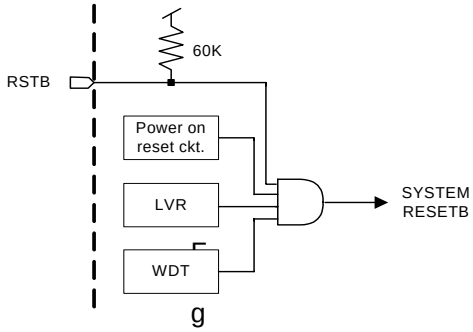
The RTC period can be pre-divided by 8 if SPUP option is disabled, and RTCFG flag will be cleared by software. This RTC timer can be used in applications that required to wake up periodically in HALT mode. The RTC clock source is come from LRCOSC oscillator and the frequency is 458.752KHZ±12%. Besides, RTC counter value also support clear function by writing “0Ah” data to register DMDM ($1DH).

Use external 32K X’tal oscillator for RTC clock source

The clock source of RTC can come from LRCOSC or EXT32K oscillator, and MCU still run 0.5 MIPS~ 16 MIPS. If precision clock time is need, the EXT32K oscillator can be enabled by XT32ENB option. The detail clock structure of RTC is shown in Figure 7. The 32K X’tal must be connected to XIN/PB1 and XOUT/PB0 pin. To eliminate external crystal capacitor, TR4P271AT/AF provides built-in capacitor for external X’tal by VC10P option.

5.13 Reset

The actual system reset of this chip combines with four signals, which are power on reset, low voltage reset (LVR), external RSTB pin and WDT overflow reset. A dedicated RSTB pin (shared with PA3) can be used to reset TR4P271AT/AF externally. This pin has internal 60K ohm pull up resistor. MCU will go to NORMAL mode when RSTB occurred in HALT mode.



g
u
Figure 15

5.14 Low Voltage Reset

When VDD power is applied to the chip, the low voltage RSTB default is enabled initially, it will be disabled when in HALT mode. The internal system reset will be generated if VDD is lower than V_{LVR}.

5.15 System Clock Oscillator

The TR4P271AT/AF is provided with an internal high speed RC oscillator (HRCOSC) that provided a precision frequency of deviation under ±2% for VDD from 2.0V to 5.5V and temperature from -40℃ to +85℃. An internal low speed RC oscillator (LRCOSC) and an external X'tal oscillator or ceramic resonator (EXTOSC) are provided also. This chip is a dual clock MCU system. In NORMAL mode, MCU operating clock (F_{MCK}) comes from HRCOSC or EXTOSC. In GREEN mode, clock source come from LRCOSC.
Condition VDD=2.0V~5.5V

TYPE	OSC frequency	MCU clock (F_{MCK})	MCU operation mode
HRCOSC	(1) 32MHz ±2% (2) 32MHz -16%~+10% by PB0/OSCADJ pin (3) 32MHz -2%, +2%, -4%, +4% by HRC_ADJ register	F_{HRCOSC}/2, /4, /8, /32 (MCU run 16 MIPS/8 MIPS/4 MIPS/1 MIPS by option)	NORMAL mode
EXTOSC	X'tal 455KHz~32MHz	F_{XTOSC} / 2 , F_{XTOSC} / 4, F_{XTOSC} / 8, F_{XTOSC} / 16	NORMAL mode
LRCOSC	458.752KHz±12%	F_{LRCOSC}/4, /8, /16, /32 (MCU run at 114.69KIPS /57.34KIPS /28.67KIPS /14.33KIPS by option)	GREEN mode (low power consumption)

Table 14

System clock can be stopped by HALT command. Once stopped, only wake-up triggering inputs (PA0~PA3, PB0~3 or PD0~PD3), RSTB (if PA3 set as RSTB by option) or RTC overflow can re-start oscillator. Such oscillator will do 'stable check' before release control to software. There are 2 stable clock delays as shown in the table of page 7. This delay is placed between oscillator starting and first instruction of user software.

EXTOSC: External X'tal oscillator, XIN and XOUT are shared with PB1 and PB0 by option. An external ceramic resonator or crystal of 455KHz~16MHz can be used for MCU clock source. Due to the frequency of X'tal oscillator support wide range, so it is divided into 3 segments by option HSEN and LSEN. The X'tal oscillator option is as shown below:

X'TAL oscillator option

HSEN	LSEN	X'tal
0	0	455KHz~1MHz
0	1	2MHz~16MHz
1	0	20MHz~32MHz

Table 15

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The external X'tal oscillator also supports 32KHz crystal if option XT32ENB is enabled. It provides clock source for RTC and WDT, but don't provide clock source for MCU. The MCU is still running with internal RC oscillator in this mode.
It can be also driven by external clock in this mode. In such case, no crystal or resonator is needed. The three connection types are shown as follows:
TR4P271AT/AF provides built-in capacitor for external X'tal. If option VC10P is disabled, Cap.C1 and C2 use 10P~20P for 32K X'tal, and 20P for 1~16 MHz X'tal. If option VC10P is enabled, C1 and C2 don't need for 1~12MHz except 16MHz X'tal.

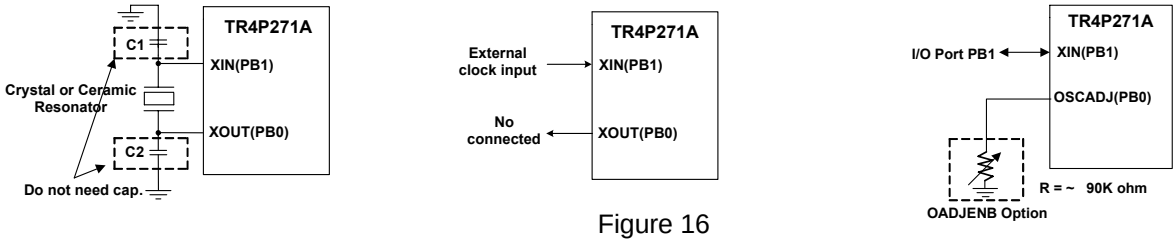


Figure 16

HRCOSC: Internal high speed RC oscillator, the frequency of this oscillator can be adjusted by external OSCADJ (PB0) pin which is selected by option if need. When OSCADJ pin is used for frequency adjust, it must be connected to a resistor and then serial to VSS. The recommended resistor value is from 0 ohm to 90K ohm and the frequency range built around 32MHz -16% ~ +10%. There is one measurement data as shown below:
Table 16

OSCADJ PIN resistor (KΩ)	0K	10K	20K	30K	43K	51K	62K	75K	82K	91K
HRCOSC frequency deviation	-19%	-6.5%	0%	+4.5%	+7.5%	+8.8%	+10%	+11.8%	+12.2%	+13%

Note: This data is only for reference. It has some frequency deviation due to process variation, temperature and operating voltage.

There is another frequency adjustment method on HRCOSC. Using IADJEN, ADJ1, and ADJ0 control register, the frequency of 32MHz can shift +2%, -2%, +4% or -4% four kinds of frequency deviation. Special care must be taken by user when this method is applied, the device would not guarantee frequency deviation range for different chips. These four kinds of frequency deviation is only reference value.

HRC_ADJ	04H	R/W	0000	X	IADJEN	ADJ1	ADJ0	IADJEN: HRCOSC internal adjust on/off 0: HRCOSC internal adjust disabled 1: HRCOSC internal adjust enabled ADJ1,ADJ0: HRCOSC internal adjust reg.

ADJ1	ADJ0	Internal HRCOSC frequency
0	0	32MHz + 4%
0	1	32MHz + 2%
1	0	32MHz - 2%
1	1	32MHz - 4%

5.16 I/O Port (input/output)

TR4P271AT/AF provides totally 11 I/O ports and one input port. There are three bi-direction I/O port, Port A ,Port B, and Port D. Input and output direction is controlled by IOC_PA, IOC_PB, IOC_PD. All I/O are provided with wake up and pull down/up resistor function by control registers.

5.16.1 PortA /PortB (input/output)

Common I/O

Symbol	Addr.	R/W	RSTB	D3	D2	D1	D0	Description
IOC_PA	02H	R/W	0000	X	**IOCA2**	**IOCA1**	**IOCA0**	Port PA0~PA2 input/output direction : 1: set port as output port individually 0: set port as input port individually PA3 is input only.
DATA_PA	03H	R/W	xxxx	**DPA3 (Read only)**	**DPA2**	**DPA1**	**DPA0**	Read data from PA0~PA3 PIN or write data to PA0~PA2 PIN (I/O direction is selected by IOC_PA register)
IOC_PB	05H	R/W	0000	**IOCB3**	**IOCB2**	**IOCB1**	**IOCB0**	Port PB0~PB3 input/output direction : 1: set port as output port individually 0: set port as input port individually
DATA_PB	06H	R/W	xxxx	**DPB3**	**DPB2**	**DPB1**	**DPB0**	Read data from PB0~PB3 port or write data to PB0~PB3 (I/O direction is defined by IOC_PB register)

Extend I/O

Symbol	Addr.	R/W	Reset	D3	D2	D1	D0	Description
PAPU	00H	W	0000	**PAPU.3**	**PAPU.2**	**PAPU.1**	**PAPU.0**	PA2~PA0 pull up 100K ohm resistor PA3 pull up 60K ohm resistor 0: Port A pull up resistor disabled 1: Port A pull up resistor enabled
PAPL	01H	W	0000	**PAPL.3**	**PAPL.2**	**PAPL.1**	**PAPL.0**	Port A pull down 100K ohm resistor 0: Port A pull down resistor disabled 1: Port A pull down resistor enabled
PBPU	02H	W	0000	**PBPU.3**	**PBPU.2**	**PBPU.1**	**PBPU.0**	Port B pull up 100K ohm resistor 0: Port B pull up resistor disabled 1: Port B pull up resistor enabled
PBPL	03H	W	0000	**PBPL.3**	**PBPL.2**	**PBPL.1**	**PBPL.0**	Port B pull down 100K ohm resistor 0: Port B pull down resistor disabled 1: Port B pull down resistor enabled
PAWK	06H	W	0000	**PAWK.3**	**PAWK.2**	**PAWK.1**	**PAWK.0**	Port A wake up enable control 0: Port A wake up disabled 1: Port A wake up enabled
PBWK	07H	W	0000	**PBWK.3**	**PBWK.2**	**PBWK.1**	**PBWK.0**	Port B wake up enable control 0: Port B wake up disabled 1: Port B wake up enabled

The Port A and Port B are 4-bit I/O port. Each bit (pin) can be individually set as input port or output port. In output mode, data can be written to external pin. In output mode, data read will read internal register data not external pin voltage. External pull-up/down resistor will be disabled when in output mode.
In input mode, Port A and Port B data is read voltage on external pin. These pins can have pull-up/down resistor 100K or not. They are selected by PAPU, PAPL, PBPU, PBPL registers. The pull up resistor of PA3 isn't 100k, it's 60K ohm only.
Each pin of Port A and Port B can be selected with wake up function or not by register PAWK or PBWK. In HALT mode, If Port A or Port B wake-up function is enabled. Any rising or falling signal on these selected ports will wake up system and turn on HRCOSC or EXTOSC oscillator simultaneously. Program counter of MCU will jump to Address 04H to run wake up program.
When Port A and Port B is selected as wake-up enabled, and system enters HALT mode by HALT instruction. Then, these ports will automatically enter input mode even if they are set as output ports previously. This function is not provided for Port D and PA3.

PA1 is provided with 38KHz modulator

I/O port PA1 can be used as 38KHz modulator output. This function is enabled by **F38K** modulator option. PA1 pin will output 38KHz clock signal when F38K set to 1 (PA1 always as output port when IREN option enabled). If register F38K set to 0, PA1 output keeps low or high depend on option IRNOR0. See below for detail. If this 38K modulator option is disabled, PA1 will be changed to normal I/O port.

No.	IRNOR0 option	F38K register	PA1 output pin
1	disabled	0	low
2	disabled	1	38k square wave
3	enabled	0	high
4	enabled	1	38k square wave

Table 17

This 38KHz modulator has several clock sources under different modes as shown below:

MCU mode	NORMAL mode		GREEN mode
Clock source	Use internal HRCOSC	Use external X'tal oscillator Use 16MHz X'TAL is a must	Use internal LRCOSC
38K frequency	F_{HRCOSC} /840 = 38.09±2%KHz	F_{XTOSC}=16Mhz/420 = 38.09KHz	F_{LRCOSC}/12 = 38.23±12% KHz

Table 18

Symbol	Addr.	R/W	Reset	D3	D2	D1	D0	Description
RTC	01H	R/W	0000	RTCFG	**F38K**	RTCS1	RTCS0	F38K is valid only when IREN is enabled. F38K = 1, PA1 output 38k clock F38K = 0, PA1 PIN 38K output signal disabled. PA1 keeps low if (option) IRNOR0 disabled. PA1 keeps high when IRNOR0 enabled.

PA0 is shared with AN2 pin by option.
PA1 is shared with AN1/IR38K functions by option
PA2 is shared with AN0/BZ/CKI functions by option
PA3 is an input pin only, with pull up 60K and pull down resistor 100K ohm. It also provides level changed wake up function. It's shared with external reset pin (RSTB) pin by option, and VPP pin (VPP is for programming only).
PB0 is shared with XOUT/OSCADJ/PWM3H by option and PB1 is shared with XIN pin by option. XIN and XOUT PIN can be connected to external crystal to replace internal oscillator HRCOSC. Once XTENB option is enabled, the pull up/down control registers and I/O direction registers of these two PINs will be disabled.
PB2 is shared with output of Op Amp by option.
PB1 is shared with XIN/PWM3L functions by option.
PB2 is shared with an output of Op Amp (CA3)/PWM2H functions by option.
PB3 is shared with AN3/EINTB/BRAKE functions.
Notice: The external interrupt and brake function is not provided in GREEM mode.

PA0~PA2 and PB3 are shared with ADC's input AN2~AN0 and AN3
If the PA0 is used as AN2 input, PA2 must set as input mode. Besides, in order to avoid leakage current occur, the pull up/down registers PAPU.0 and PAPL.0 must be set to 1 so that input circuit is disabled. These two pull up/down registers enabled simultaneously is a special control method for ADC's input, any pull up/down resistor isn't enabled. The same control method is used on PA1/AN1, PA2/AN0 and PB3/AN3 also.

5.16.2 PortD (input/output)

Common I/O

Symbol	Addr.	R/W	RSTB	D3	D2	D1	D0	Description
IOC_PD	0CH	R/W	0000	**IOCD3**	**IOCD2**	**IOCD1**	**IOCD0**	Port D input/output direction select 1: set port as output port individually 0: set port as input port individually
DATA_PD	0DH	R/W	xxxx	**DPD3**	**DPD2**	**DPD1**	**DPD0**	Read port D data from PD0~PD3 port or write data to PD0~PD3 (I/O direction is defined by IOC_PD register)

Extend I/O

Symbol	Addr.	R/W	Reset	D3	D2	D1	D0	Description
PDPU	04H	W	0000	**PDPU.3**	**PDPU.2**	**PDPU.1**	**PDPU.0**	Port D pull up 100K ohm resistor 0: Port D pull up resistor disabled 1: Port D pull up resistor enabled
PDPL	05H	W	0000	**PDPL.3**	**PDPL.2**	**PDPL.1**	**PDPL.0**	Port D pull down 100K ohm resistor 0: Port D pull down resistor disabled 1: Port D pull down resistor enabled
PDWK	08H	W	0000	**PDWK.3**	**PDWK.2**	**PDWK.1**	**PDWK.0**	Port D wake up enable control 0: Port D wake up disabled 1: Port D wake up enabled

IOC_PD register defines the input/output selection of PD0~PD3.
PDWK register defines wake up function of PD0~PD3.
PDPU/PDPL defines the existence of 100K resistor pull up/down in input mode, just like Port A or Port B.
Notice: If Port D pins are wakeup-enabled and is set as output port by software, and if system enters HALT mode, it will not automatically change to input mode (as port A and port B). It will keep as output. Only Port A and Port B is provided with this function.

Figure 17

PD0, PD1, PB2 are shared with input/output of OP Amp.
There is one OP Amp in TR4P271AT/AF. The input/output pin of this OP Amp are shared with PD0, PD1 and PB2 pin by option. If OP Amp is enabled, the register DPD0 and DPD1 will always read 0. The I/O direction register of PD0, PD1 and PB2 are ignored. Pull up or down resistors are still available. This OP Amp will be automatically powered down in HALT mode.

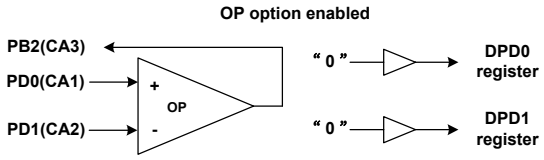
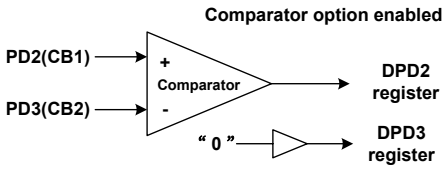


Figure 18

PD2, PD3 are shared with input of a Comparator
There is one comparator in TR4P271AT/AF. The input pin of comparator are shared with PD2 and PD3 pin by option. If the comparator option is enabled, the connection of external pin, internal register and comparator are as shown in the figure right. The output of comparator is connected to register DPD2, and register DPD3 is always fixed to 0 in this mode. The I/O direction register of PD2 and PD3 are ignored (PD2 and PD3 will be forced as input port by hardware). Pull up or down resistors are still available. This comparator will be automatically powered down in HALT mode.



PD2 and PD3 are shared with ADC's input AN5 and AN4
If the PD2 is used as AN5 input, PD2 must set as input mode. Besides, in order to avoid leakage current occur, the pull up/down registers PDPU.2 and PDPL.2 must be set to 1 so that input circuit is disabled. These two pull up/down registers enabled simultaneously is a special control method for ADC's input, any pull up/down resistor isn't enabled. The same control method is used on PD3/AN4 also.

5.17 12bits Analog to Digital Converter (ADC)

The need to interface to real world analog signals is a common requirement for many electronic systems. However, to properly process these signals by a MCU, they must first be converted into digital signals by ADC. By integrating the ADC electronic circuitry into the MCU, the need for external components is reduced significantly with the corresponding follow-on benefits of lower costs and reduced component space requirement.

ADC Overview

TR4P271AT/AF contains a 6-channel analog to digital converter using multiplexed to ADC. The device can directly interface to external analog signals, such as sensors or other control signals and convert these signals to a 12-bit binary presentation of that signal. Besides, it provides temperature sensor and bandgap reference voltage generator. These two sensors are internally connected to multiplexer of the ADC's AN6. Refer to the picture is as shown below.

The accompanying block diagram shows the overall internal structure of the ADC, together with its associated registers.

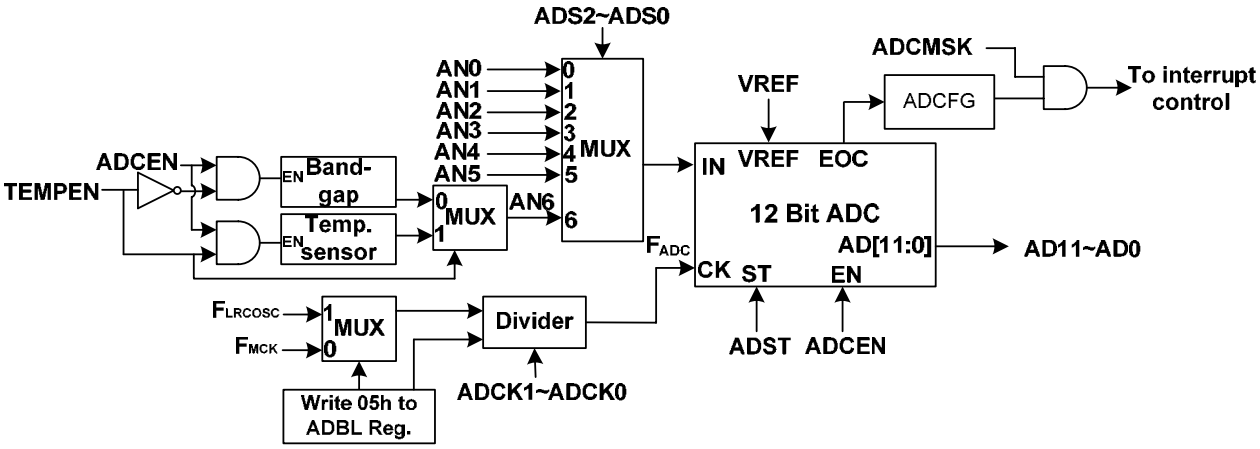


Figure 19. ADC block diagram

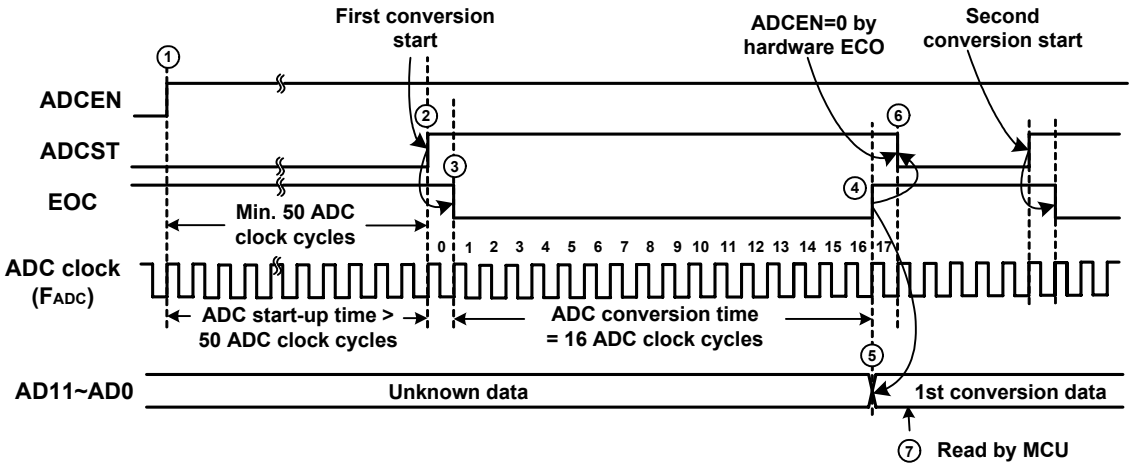


Figure 20. A/D conversion timing

Symbol	Addr.	R/W	RSTB	D3	D2	D1	D0	Description
ADCCTL	11H	R/W	0000	**TEMPEN**	**ADCEN**	**ADCST**	**EOC (R)**	EOC: End of A/D conversion 0: A/D conversion in process 1: A/D conversion is completed, the ADCST bit is automatically cleared when EOC rising edge occurred. ADCST: To start A/D conversion 0: A/D conversion not in progress 1: to start A/D conversion ADCEN: ADC converter enable control 0: ADC disabled, no operating current. 1: ADC enabled TEMPEN: Temperature sensor and bandgap enabled control 0: Temperature sensor disabled and bandgap voltage generator enabled 1: Temperature sensor enabled and bandgap voltage generator disabled
CHSEL	12H	R/W	0111	**BRKEN**	**ADS2**	**ADS1**	**ADS0**	BRKEN: PWM brake function enable 0: PWM brake function disabled 1: PWM brake function enabled ADS2~ADS0: ADC channel selection
ADCCKS	13H	R/W	0000	**ADCMSK**	**ADCFG**	**ADCK1**	**ADCK0**	ADC clock source selection table ADCFG: ADC interrupt flag 0: no ADC interrupt occurred 1: ADC interrupt occurred ADCMSK: ADC interrupt mask 0 : ADC interrupt mask enabled, ADC interrupt disabled. 1: ADC interrupt mask disabled, ADC interrupt enabled.

ADS2	ADS1	ADS0	Channel
0	0	0	AN0
0	0	1	AN1
0	1	0	AN2
0	1	1	AN3
1	0	0	AN4
1	0	1	AN5
1	1	0	AN6 (for bandgap or temperature sensor)
1	1	1	All ANn disabled

ADCK1	ADCK0	ADC clock source
0	0	FMCK /2(or FLRCOSC /1)
0	1	FMCK /4(or FLRCOSC /2)
1	0	FMCK /8(or FLRCOSC /4)
1	1	FMCK /16(or FLRCOSC/8)

Extend I/O

Symbol	Addr.	R/W	Reset	D3	D2	D1	D0	Description
ADBH	09H	R	xxxx	**AD11**	**AD10**	**AD9**	**AD8**	AD11(MSB)~AD0(LSB) : 12bit ADC converter result. **Note: The clock of ADC would be changed to LRCOSC(458KHz) by writing data 05h to ADBL register. It's would be changed back by writing the others data (except 05h).**
ADBM	0AH	R	xxxx	**AD7**	**AD6**	**AD5**	**AD4**	
ADBL	0BH	R/W	xxxx	**AD3**	**AD2**	**AD1**	**AD0**	

ADC Data Registers (ADBH, ADBM, ADBL)

TR4P271AT/AF is provided an internal 12-bit ADC. It requires three nibble registers, a high nibble register, known as ADBH, a middle nibble register, known as ADBM and low nibble register, known as ADBL. After A/D conversion process takes place, the 12 bits result stored in these registers. They can be directly read by the MCU to obtain the digitized conversion value. In the table above, AD11~AD0 is the A/D conversion result.
Note: The clock of ADC can be changed to FLRCOSC (458KHz) by writing data 05h to ADBL register. It's can be changed back by writing others data except 05h.

ADC channel selection Register (CHSEL)

The ADC input channel AN0~AN5 are shared with PA2~PA0, PB3, PD3, PD2 pin. Any specified I/O ports are used as ADC input channel, these I/O port must be set as input mode by program. The input circuit of specified I/O port faces analog signal input, current leakage will be increased. So, in order to avoid current leakage in input port, the ADC input channel must be configured by using its pull up and pull down resistor are all enabled. In this condition, regardless of the pull up and pull down resistors will be all enabled actually. The AN0~AN5 must be connected to 0.1uF capacitor if it's applied as ADC's input channel.

ADC Control Register (ADCCTL)

The ADC function is enabled by setting ADCEN bit to 1. The ADC is disabled and consumes no operating current by setting ADCEN bit to 0. In order to save power consumption in HALT Mode, **the ADCEN bit must be cleared to 0 before into HALT Mode**.
The ADCST bit of the ADCCTL register is used to start the A/D conversion. When the MCU sets this bit from 0 to 1, an analog to digital conversion cycle will be initiated. Special care must be taken by the user when ADCST bit is set to 1. **The ADC start-up delay time consists of 50 ADC clock (FADC) cycles, and it must be inserted between ADCEN and ADCST set to 1.** During A/D conversion, the EOC bit is clear to 0. After 16 ADC clock cycles, the EOC bit will be set to 1 and the ADCST bit will be automatically cleared to 0 by circuit. The ADCST bit is used to control the overall start operation of the A/D conversion. The EOC bit is used to indicate when the A/D conversion process is completed, and it will be automatically set to 1 by circuit after a conversion cycle has completed. In addition, if the global interrupt is enabled (ENINT=1) and ADCMSK is set to 1, an interrupt request flag ADCFG will be set when A/D conversion has completed. This ADC interrupt signal will direct the program flow to interrupt Address ($008h) for processing. If the ADC interrupt is disabled, the MCU can use polling the EOC bit to check whether it has been completed or not. It's an alternative method of detecting the end of an A/D conversion cycle.

ADC clock source selection (ADCCKS)

The clock source of the ADC (FADC) originates from two sources, the system clock FMCK or FLRCOSC. After system reset, the clock source of ADC comes from FMCK. It can be changed to LRCOSC (458KHz) by writing data 05h to ADBL register, and changed back by writing the others data (except 05h).
If clock source of the ADC comes from FMCK, it's first divided by a pre-scaler which is determined by the ADCK1 and ADCK0 bits in the ADCCKS register. Although the ADC clock source is determined by the system clock FMCK, ADCK1 bit and ADCK0 bit, there are some limitations on the maximum ADC clock speed that can be selected. As the minimum value of permissible ADC clock period Tad is 0.25us, care must be taken for system clock speeds in excess of 16MHz. For system clock speeds in excess of 16MHz, the ADCK1 and ADCK0 bits should not be set to "00". Doing so will give ADC clock periods that are less than the minimum ADC clock period (0.25us) which may result in inaccurate ADC values. Refer to the following Table 17, where values marked with an asterisk "*" show where depending upon the device, special care must be taken as the values may be less than the specified minimum ADC clock period.
FADC comes from FMCK

ADC clock definition (FADC)			ADC clock period (Tad) vs. MCU clock speed (FMCK)			
ADCK1	**ADCK0**	ADC clock source	MCU run 1 MIPS	MCU run 4 MIPS	MCU run 8 MIPS	MCU run 16 MIPS
0	**0**	FMCK /2	2us	0.5us	0.25us	* 0.125us
0	**1**	FMCK /4	4us	1us	0.5us	0.25us
1	**0**	FMCK /8	8us	2us	1us	0.5us
1	**1**	FMCK /16	16us	4us	2us	1us

Table 19

Notice: Don't use Tad marked with the asterisk "*" clock period for A/D conversion.

If clock source of the ADC comes from F_{LRCOSC}, it's first divided by a pre-scaler which is determined by the ADCK1 and ADCK0 bits in the ADCCKS register. In this mode, the Table 20 shows the ADC's clock don't affect by different MCU operation speed.

F_{ADC} comes from F_{LRCOSC}

ADC clock definition (F_{ADC})			ADC clock period (Tad) vs. MCU clock speed (F_{MCK})
ADCK1	**ADCK0**	ADC clock source	MCU run 1~16 MIPS
0	**0**	F_{LRCOSC} /1	2.18us ±12%
0	**1**	F_{LRCOSC} /2	4.36us ±12%
1	**0**	F_{LRCOSC} /4	8.73us ±12%
1	**1**	F_{LRCOSC} /8	17.46us ±12%

Table 20

AVSS and VREF PIN

The ADC's input range is limited by the VREF voltage and AVSS. The VREF voltage comes from external VREF pin or bonding to VDD in package. The VREF pin should be connected to VDD or smaller than VDD voltage supply, and it must be connected to 0.1uf capacitor. The voltage of ADC's result AD[11:0] can be calculated by equation below:

V_{ANn} = VREF X AD[11:0]/4096 (n = 0 ~ 5)

For more precision ADC requirement and low noise performance, theTR4P271 series support AVSS and VREF pin on SOP16 package. Special care must be taken by the user when using SOP16 package. The AVSS pin on PCB must be connected to external ground as short as possible.

Notice: The PCB layout of VREF pin to power must be carefully with low noise interference.

5.18 On chip Temperature sensor and Bandgap reference voltage

TR4P271AT/AF provides an internal temperature sensor for temperature control and a bandgap reference voltage for low battery detection. They can be enabled by ADCEN set to 1 and use TEMPEN bit of ADCCTL register to select which one is enabled.

In order to make these two special functions have enough stable time on interface with ADC, the clock period Tad of ADC must not be smaller than 1us. Refer to table21 is as shown below.

ADC clock definition (F_{ADC})			ADC clock period (Tad) vs. MCU clock speed (F_{MCK})			
ADCK1	**ADCK0**	ADC clock source	MCU run 1 MIPS	MCU run 4 MIPS	MCU run 8 MIPS	MCU run 16 MIPS
0	**0**	F_{MCK}/2	2us	* 0.5us	* 0.25us	* 0.125us
0	**1**	F_{MCK} /4	4us	1us	* 0.5us	* 0.25us
1	**0**	F_{MCK} /8	8us	2us	1us	* 0.5us
1	**1**	F_{MCK} /16	16us	4us	2us	1us

Table 21

Notice: Don't use Tad marked with the asterisk "*" clock period when temperature sensor and bandgap reference voltage generator is enabled.

Symbol	Addr.	R/W	Reset	**D3**	**D2**	D1	D0	Description
ADCCTL	11H	R/W	0000	**TEMPEN**	**ADCEN**	ADCST	EOC (R)	ADCEN: ADC converter power on/off 0: ADC power down 1: ADC power on TEMPEN: Temperature sensor enabled / disabled control 0: Temperature sensor disabled and bandgap voltage generator enabled 1: Temperature sensor enabled and bandgap voltage generator disabled

5F-2, No. 83, Sec. 2, Gongdao 5th Rd., HSIN-CHU, TAIWAN, R.O.C. TEL: 886-3-5160191 FAX: 886-3-5160233 Web site: www.tritan.com.tw

5.18.1 On chip Bandgap Reference Voltage

The bandgap reference voltage is suitable for low battery detection. It can be enabled by setting TEMPEN register to 0 and select AN6 as ADC's input by ADS2~ADS0 bits as 110. The operation procedure is as shown below:

1. Clear TEMPEN and ADCFG bits to 0.
2. Set ADS2~ADS0 to 110.
3. Select ADC conversion clock by setting ADCK1 and ADCK0 register..
4. Turn on ADC module by setting ADCEN to 1.
5. Delay over 100us and 50 cycles of ADC clock, these two delays must be fit for bandgap reference voltage and ADC start-up time.

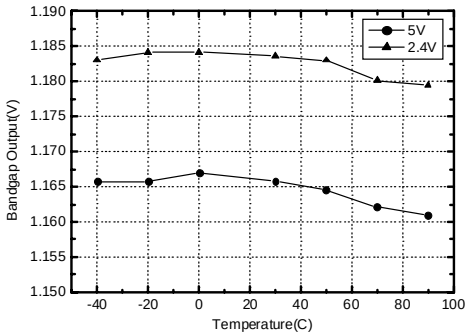


Figure 21. Temperature V.S. Bandgap Output(Vout)

6. Start conversion by setting ADCST to 1.
7. Check the end of A/D conversion by follows:
   (a) Polling for the EOC bit to be set.
   (b) Polling for the ADCFG bit to be set.
   (c) Wait for the interrupt from ADCFG set to 1.
8. If A/D conversion is completed, read 12 bits A/D conversion result from AD11~AD0 bits. This value represents the bandgap reference voltage.

The start-up time of bandgap reference voltage (Tbg) must greater than 100us, it is shown in the section 4. AC characteristic table. Due to temperature, VDD and process variation, the bandgap reference voltage will vary from chip to chip around 1.175 **±** 4%V , temp.= -40°C ~+85°C . Base on different VDD voltage, the temperature curve of bandgap is shown above:

5.18.2 On chip Temperature sensor

A on-chip temperature sensor is integrated within AN6 and provides temperature sensing capability of -40°C~ 85°C. The accuracy of the temperature sensor is approximately ± 6°C. The temperature sensor develops an output voltage proportional to temperature with a temperature coefficient of 2.8 LSB/°C or 3.3 LSB/°C.
In order to make temperature sensor more accurate, a Temperature Calibration Value (TCV) is stored in Address $670h. Once ADC transform has been completed, the user will need to calculate the temperature using these two coefficients. If ADC's conversion output data is greater than TCV, then use temperature coefficient of 3.3 LSB/°C as shown below formula 1. Otherwise, use temperature coefficient of 2.8 LSB/°C as shown below formula 2.

$$Temperature = 27°C + \frac{(12bit\_ADC\_output - TCV)}{3.3}$$ ------ formula 1

$$Temperature = 27°C - \frac{(TCV - 12bit\_ADC\_output)}{2.8}$$ ------ formula 2

The chip temperature can be calculated from its temperature coefficient and Temperature Calibration Value (TCV). The TCV is an A/D conversion value which measured at 27℃, and stored on OTP Address $670h during mass production processing. Each chip has its own TCV for process variation.

For example, if ADC conversion result is 89Eh, and the TCV code assume 850h. Because ADC result is greater than the TCV, so choose the formula 1 to calculate chip temperature. After calculating, the chip temperature is 50.6°C (27°C + (89Eh-850h)/3.3).

To use the temperature sensor, the user must perform following:

1. Set TEMPEN to 1 and ADCFG bits to 0.
2. Set ADS2~ADS0 to 110.
3. Select ADC conversion clock by setting ADCK1 and ADCK0 register..
4. Turn on ADC module by setting ADCEN to 1.
5. Delay over 50 ADC cycles, this delay must be fit for ADC start-up time.
6. Start conversion by setting ADCST to 1.
7. Check the end of A/D conversion by follows:
   (a) Polling for the EOC bit to be set.
   (b) Polling for the ADCFG bit to be set.
   (c) Wait for the interrupt from ADCFG set to 1.
8. If A/D conversion is completed, the 12 bits A/D conversion result is stored in AD11~AD0 bits. The chip temperature can be obtained from calculating this result and TCV.

6. Application Circuit

PCB Layout guide line for 32K Crystal

Notice:

1. The overall shield track must be placed around the 32k crystal.
2. The 32k crystal must be placed close to XIN & XOUT pin (< 0.5cm is perfect)
3. Ground “path A”and “path B”must be separated.

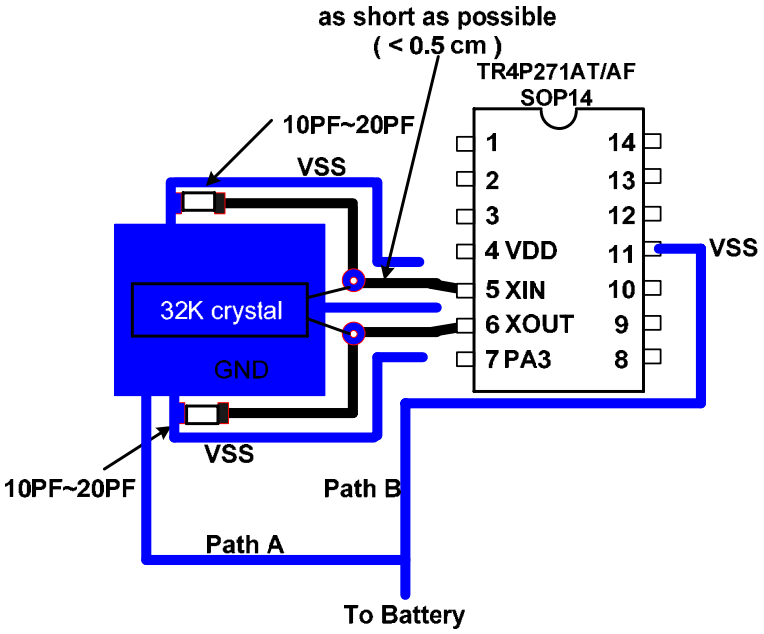
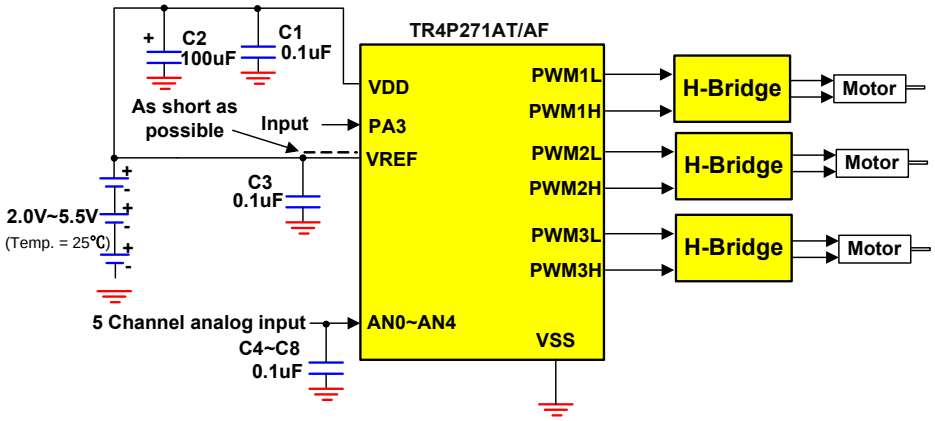
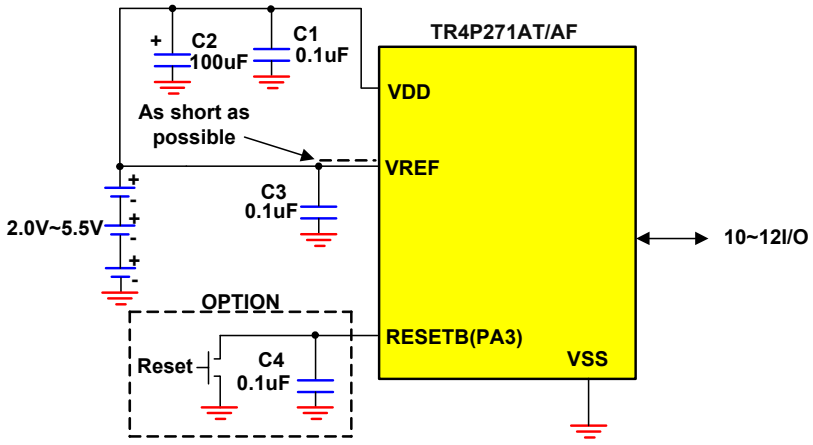


Figure 22



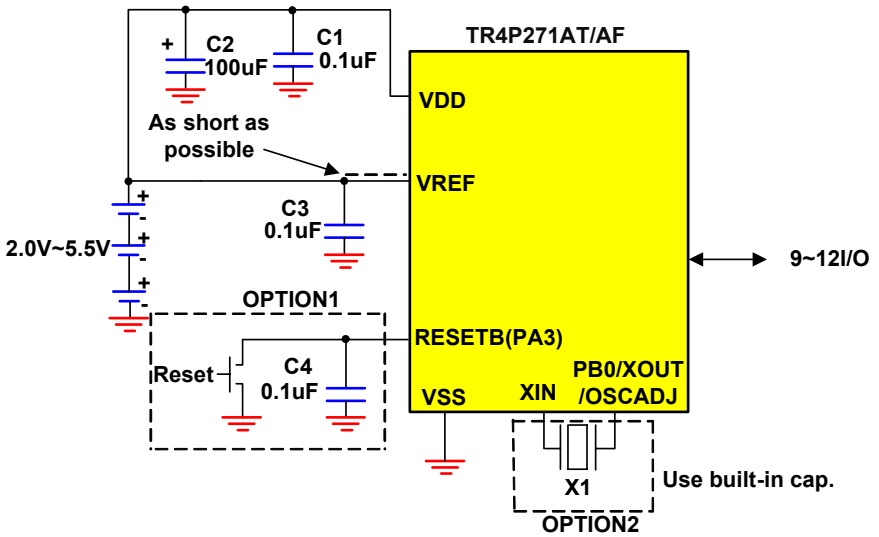
Note : Substrate must be connected to VSS.

Figure 23



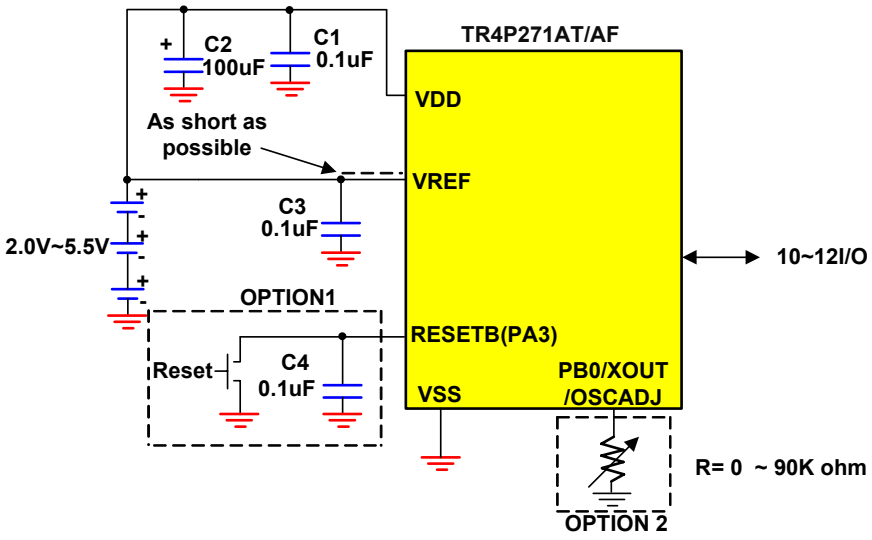
Note : Substrate must be connected to VSS.

Figure 24



Note : Substrate must be connected to VSS.

Figure 25



Note : Substrate must be connected to VSS.

Figure. 26

7. Option Registers table

<table>
<tr><th>Item</th><th>Option Name</th><th>Function Description</th></tr>
<tr><td>1</td><td>PA3_RESETB</td><td>Enable/disable RSTB (PA3 pin is shared with RSTB.)</td></tr>
<tr><td>2</td><td>WDT</td><td>WDT enable/disable</td></tr>
<tr><td>3</td><td>XTENB</td><td>External crystal mode enable/disable</td></tr>
<tr><td>4

5</td><td>MCKS1

MCKS0</td><td>MCU operating clock definition (F_{MCK})
(external crystal frequency= F_{XTOSC})
<table>
<tr><th>ITEM</th><th>Option XTENB=1
Use internal HRCOSC</th><th>Option XTENB=0
Use external EXTOSC
(F_{XTOSC})</th></tr>
<tr><td>1</td><td>MCU run 16MHz</td><td>X</td></tr>
<tr><td>2</td><td>MCU run 1MHz</td><td>MCU run F_{XTOSC} /16</td></tr>
<tr><td>3</td><td>MCU run 4MHz</td><td>MCU run F_{XTOSC} /4</td></tr>
<tr><td>4</td><td>MCU run 8MHz</td><td>MCU run F_{XTOSC} /2</td></tr>
</table></td></tr>
<tr><td>6</td><td>PROTECT</td><td>OTP data lock bit enabled/disabled</td></tr>
<tr><td>7</td><td>IREN</td><td>Enable/disable IR 38K (PA1 is shared with IR 38K clock output.)</td></tr>
<tr><td>8</td><td>WDTHEN</td><td>WDT always enabled or not, even in HALT mode.</td></tr>
<tr><td>9

10</td><td>WDTS1

WDTS0</td><td>WDT period definition
<table>
<tr><th>ITEM</th><th>WDT Period</th></tr>
<tr><td>1</td><td>0.125 ±12% Sec</td></tr>
<tr><td>2</td><td>0.25 ±12% Sec</td></tr>
<tr><td>3</td><td>0.5 ±12% Sec</td></tr>
<tr><td>4</td><td>1.0 ±12% Sec</td></tr>
</table></td></tr>
<tr><td>11

12</td><td>LOSCS1

LOSCS0</td><td>MCU operating clock definition in GREEN Mode
<table>
<tr><th>ITEM</th><th>MCU GREEN mode clock</th></tr>
<tr><td>1</td><td>114.69 ±12% KIPS</td></tr>
<tr><td>2</td><td>57.34 ±12% KIPS</td></tr>
<tr><td>3</td><td>28.67 ±12% KIPS</td></tr>
<tr><td>4</td><td>14.33 ±12% KIPS</td></tr>
</table></td></tr>
<tr><td>13</td><td>IRNOR0</td><td>PA1 pin keep high or low when option IREN enabled and F38K register = 0 (38K stopped)
<table>
<tr><th>No.</th><th>IRNOR0 option</th><th>F38K register</th><th>PA1 output pin</th></tr>
<tr><td>1</td><td>disabled</td><td>0</td><td>low</td></tr>
<tr><td>2</td><td>disabled</td><td>1</td><td>38k square wave</td></tr>
<tr><td>3</td><td>enabled</td><td>0</td><td>high</td></tr>
<tr><td>4</td><td>enabled</td><td>1</td><td>38k square wave</td></tr>
</table></td></tr>
<tr><td>14</td><td>RTCEN</td><td>Enable/disable RTC function</td></tr>
<tr><td>15</td><td>OADJENB</td><td>PB0 is shared with OSCADJ PIN (Adj. pin of HRCOSC) or not</td></tr>
<tr><td>16</td><td>OPEN</td><td>Enable/disable OP</td></tr>
<tr><td>17</td><td>CMPEN</td><td>Enable/disable Comparator</td></tr>
<tr><td>18</td><td>XT32ENB</td><td>Enable/disable 32K X'tal oscillator</td></tr>
<tr><td>19</td><td>SPUP</td><td>Enable/disable RTC time period speed up.</td></tr>
<tr><td>20

21</td><td>LVRS1

LVRS2</td><td>
<table>
<tr><th>LVRS3</th><th>LVRS2</th><th>LVRS1</th><th>LVR voltage level</th></tr>
<tr><td>0</td><td>0</td><td>0</td><td>x</td></tr>
<tr><td>0</td><td>0</td><td>1</td><td>x</td></tr>
<tr><td>0</td><td>1</td><td>0</td><td>LVR level = 1.7V</td></tr>
</table></td></tr>
</table>

<table>
<tr><td>22</td><td>LVRS3</td><td>
<table>
<tr><td>0</td><td>1</td><td>1</td><td>LVR level = 1.9V</td></tr>
<tr><td>1</td><td>0</td><td>0</td><td>LVR level = 2.1V</td></tr>
<tr><td>1</td><td>0</td><td>1</td><td>LVR level = 2.3V</td></tr>
<tr><td>1</td><td>1</td><td>0</td><td>LVR level = 2.5V</td></tr>
<tr><td>1</td><td>1</td><td>1</td><td>LVR level = 2.7V</td></tr>
</table>
</td></tr>
<tr><td>23</td><td>VC10P</td><td>Built-in 10P cap. In X’TAL oscillator
VC10P=1, built-in 10P cap. in chip
VC10P=0, no built-in 10P cap. in chip</td></tr>
<tr><td>24</td><td>HSEN</td><td rowspan="2">X’TAL oscillator option
<table>
<tr><th>HSEN</th><th>LSEN</th><th>X’tal</th></tr>
<tr><td>0</td><td>0</td><td>455KHz~1MHz</td></tr>
<tr><td>0</td><td>1</td><td>2MHz~16MHz</td></tr>
<tr><td>1</td><td>0</td><td>20MHz~32MHz</td></tr>
</table>
</td></tr>
<tr><td>25</td><td>LSEN</td></tr>
</table>

8. Revision History

Version	Description	Page	Date
1.0	Established		Aug,10 2012

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