ADATA Technology Corp.

Flash memory card

Datasheet

microSDHC Class 4

Version 0.0

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Content

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1. General Description

ADATA microSDHC-Class 4 Memory Card is to save every precious, tender, and romantic moment. You may purchase high resolution digital camera, digital camcorder, or other high-end devices. However, normal Secure Digital Cards (microSDHC Cards) on the market today may not let you capture these moments because of slow read/ write speed. Slow read/write speed may cause lag time between shots, resulting in missing the opportunity to record some of your finest memories. This ADATA microSDHC -Class 4 memory card, rated a Class 4 performance card which means the card has a guaranteed read/write speed of at least 4MB/s, will reduce working time between shots. For those high-end digital devices users, ADATA microSDHC -Class 4 memory card will ensure you capturing every perfect moment!

- Targeted for portable and stationary applications.
- Capacity：4GB/8GB/16GB/32GB.
- Support microSDHC high capacity function up to 32GB of flash memory space.
- Compatible with all PC Card Services and Socket Services.
- Support Error Correcting Code (ECC) function to detect and correct errors.
- Support In System Programming (ISP) function to load the firmware.
- Support Wear Leverage function to maximize data endurance.
- Automatic error correction and retry capabilities.
- Supports power down commands and sleep modes.
- Support device with microSDHC logo.
- Speed Rate is Class 4.
- Enhanced DSC Function and Continuously Video shooting.

1.1 System Environmental Specifications

Parameter	Range	
Storage Capacity	4GB、8GB、16GB、32GB	
Operation Voltage	2.7 ~ 3.6V	
Temperature	Operation:	-25℃ ~ 85℃
	Storage:	-40℃ ~ 85℃
Moisture and Corrosion	Operation:	25℃ / 95% rel. humidity
	Storage:	40℃ / 93% rel. hum./500h
	Salt water spray:	3% NaCl/35C; 24h acc. MIL STD Method 1009
Durability	Minimum 10,000 insertion/removal cycles	
From Factor	11mm x 15mm x 1.0mm (L*W*T)	
Weight	0.25g	

2. Ordering Information

microSDHC-Class4	
CAPACITY	PRODUCT CODE
4GB	AUSDH4GCL4-B
8GB	AUSDH8GCL4-B
16GB	AUSDH16GCL4-B
32GB	AUSDH32GCL4-B

3. Pin Assignments

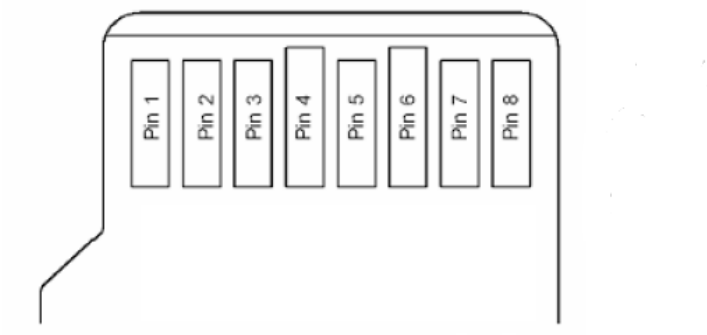


Figure 1: Contact Area

Pin #	SD Mode			SPI Mode		
	Name	Type[1]	Description	Name	Type[1]	Description
1	DAT2	I/O/PP	Data Line [Bit 2]	RSV	-	
2	CD/DAT3[2]	I/O/PP[3]	Card Detect / Data Line [Bit 3]	CS	I[3]	Chip Select (neg true)
3	CMD	I/O/PP	Command / Response	DI	I	Data In
4	VDD	S	Supply voltage	VDD	S	Supply voltage
5	CLK	I	Clock	SCLK	I	Clock
6	VSS2	S	Supply voltage ground	VSS2	S	Supply voltage ground
7	DAT0	I/O/PP	Data Line [Bit 0]	DO	O/PP	Data out
8	DAT1	I/O/PP	Data Line [Bit 1]	RSV	-	

4. System Power Consumption

General Operation Conditions

Parameter	Symbol	Min	Max	Unit	Remark
Supply Voltage	VDD	2.7	3.6	V	
Output High Voltage	VOH	0.75*VDD		V	IOH=-100uA VDD min
Output Low Voltage	VOL		0.125*VDD	V	IOL = 100uA VDD min
Input High Voltage	VIH	0.625*VDD	VDD+0.3	V	
Input Low Voltage	VIL	VSS-0.3	0.25 *VDD	V	
Power Up Time			250	ms	From 0V to VDD min
Operating Current	ICC		200	mA	IVCCF = 0mA (High speed mode)
Stand-by Current	ISB		100	uA	
Input Leakage Current	ILI		±10	uA	VIN = 0 to VDDH

5. Electrical Specifications

microSDHC			
Current Consumptions		Operate (Read / Write) :< 200 mA (High speed mode)	
		Suspend Mode : < 500uA	
Performance	Data Transfer Rates*	Performance test by HDBench (Ver3.40)	
		Read	≧ 17 MB/s
		Write	≧ 4 MB/s
System Compatibility	Windows XP,Vista , 7 , 8 , 10		
	Mac OS：10.x above		

* Note: The performance result is based on internal testing. Variations in platforms and application tools may lead to different results.

6. Card Register Information

6.1 OCR

The 32-bit operation conditions register stores the VDD voltage profile of the card. Additionally, this register includes status information bits. One status bit is set if the card power up procedure has been finished. This register includes another status bit indicating the card capacity status after set power up status bit. The OCR register shall be implemented by the cards.

The 32-bit operation conditions register stores the VDD voltage profile of the card. Bit 7 of OCR is newly defined for Dual Voltage Card and set to 0 in default. If a Dual Voltage Card does not receive CMD8,OCR bit 7 in the response indicates 0, and the Dual Voltage Card which received CMD8, sets this bit to1.

Additionally, this register includes 2 more status information bits.

Bit 31 - Card power up status bit, this status bit is set if the card power up procedure has been finished.

Bit 30 - Card capacity status bit, this status bit is set to 1 if card is High Capacity SD Memory Card. 0indicates that the card is Standard Capacity SD Memory Card. The Card Capacity status bit is valid after the card power up procedure is completed and the card power up status bit is set to 1. The Host shall read this status bit to identify a Standard or High Capacity SD Memory Card.

The OCR register shall be implemented by the cards.

OCR bit position	OCR Fields Definition
0-3	reserved
4	reserved
5	reserved
6	reserved
7	Reserved for Low Voltage Range
8	reserved
9	reserved
10	reserved
11	reserved
12	reserved
13	reserved
14	reserved
15	2.7-2.8
16	2.8-2.9
17	2.9-3.0
18	3.0-3.1
19	3.1-3.2
20	3.2-3.3
21	3.3-3.4
22	3.4-3.5
23	3.5-3.6
24-29	reserved
30	Card Capacity Status (CCS)[1]
31	Card power up status bit (busy)[2]

VDD Voltage Window

1) This bit is valid only when the card power up status bit is set.

2) This bit is set to LOW if the card has not finished the power up routine.

Table: OCR Register Definition

The supported voltage range is coded as shown in Table. A voltage range is not supported if the corresponding bit value is set to LOW. As long as the card is busy, the corresponding bit (31) is set to LOW.

6.2 CID

The Card IDentification (CID) register is 128 bits wide. It contains the card identification information used during the card identification phase. Every individual Read/Write (RW) card shall have a unique identification number. The structure of the CID register is defined in the following paragraphs:

Name	Field	Width	CID-slice
Manufacturer ID	MID	8	[127:120]
OEM/Application ID	OID	16	[119:104]
Product name	PNM	40	[103:64]
Product revision	PRV	8	[63:56]
Product serial number	PSN	32	[55:24]
reserved	--	4	[23:20]
Manufacturing date	MDT	12	[19:8]
CRC7 checksum	CRC	7	[7:1]
not used, always 1	-	1	[0:0]

Table : The CID Fields

6.2.1 MID

An 8-bit binary number that identifies the card manufacturer. The MID number is controlled, defined,and allocated to a SD Memory Card manufacturer by the SD-3C, LLC. This procedure is established to ensure uniqueness of the CID register.

6.2.2 OID

A 2-character ASCII string that identifies the card OEM and/or the card contents (when used as a distribution media either on ROM or FLASH cards). The OID number is controlled, defined, and allocated to a SD Memory Card manufacturer by the SD-3C, LLC. This procedure is established to ensure uniqueness of the CID register.

Note: SD-3C, LLC licenses companies that wish to manufacture and/or sell SD Memory Cards, including but not limited to flash memory , ROM, OTP, RAM, and SDIO Combo Cards.SD-3C, LLC is a limited liability company established by Matsushita Electric Industrial Co. Ltd., SanDisk Corporation and Toshiba Corporation.

6.2.3 PNM

The product name is a string, 5 ASCII characters long.

6.2.4 PRV

The product revision is composed of two Binary Coded Decimal (BCD) digits, four bits each, representing an “n.m” revision number. The “n” is the most significant nibble and “m” is the least significant nibble. As an example, the PRV binary value field for product revision “6.2” will be: 0110 0010b.

6.2.5 PSN

The Serial Number is 32 bits of binary number.

6.2.6 MDT

The manufacturing date composed of two hexadecimal digits, one is 8 bit representing the year(y) and the other is four bits representing the month(m).
The “m” field [11:8] is the month code. 1 = January.
The “y” field [19:12] is the year code. 0 = 2000.
As an example, the binary value of the Date field for production date “April 2001” will be: 00000001 0100.

6.2.7 CRC

CRC7 checksum (7 bits).

6.3 CSD Register

The Card-Specific Data register provides information regarding access to the card contents. The CSD defines the data format, error correction type, maximum data access time, hether the DSR register can be used, etc. The programmable part of the register (entries marked by W or E, see below) can be changed by CMD27. The types of the entries in the table below are coded as follows: R = readable, W(1) = writable once, W = multiple writable.

6.3.1 CSD_STRUCTURE

Field structures of the CSD register are different depend on the Physical Specification Version and Card Capacity.The CSD_STRUCTURE field in the CSD register indicates its structure version.Table 5-3 shows the version number of the related CSD structure.

CSD_STRUCTURE	CSD structure version	Valid for SD Memory Card Physical Specification Version/Card Capacity
0	CSD Version 1.0	Version 1.01-1.10 Version 2.00/Standard Capacity
1	CSD Version 2.0	Version 2.00/High Capacity
2-3	reserved	

Table : CSD Register Structure

6.3.2 CSD Register (CSD Version 2.0)

Table shows Definition of the CSD for the High Capacity SD Memory Card (CSD Version 2.0).The following sections describe the CSD fields and the relevant data types for the High Capacity SD Memory Card.CSD Version 2.0 is applied to only the High Capacity SD Memory Card. The field name in parenthesis is set to fixed value and indicates that the host is not necessary to refer these fields. The fixed values enables host, which refers to these fields, to keep compatibility to CSD Version 1.0. The Cell Type field is coded as follows: R = readable, W(1) = writable once, W = multiple writable.

Name	Field	Width	Value	Cell Type	CSD-slice
CSD structure	CSD_STRUCTURE	2	01b	R	[127:126]
reserved	-	6	00 0000b	R	[125:120]
data read access-time	(TAAC)	8	0Eh	R	[119:112]
data read access-time in CLK cycles (NSAC*100)	(NSAC)	8	00h	R	[111:104]
max. data transfer rate	(TRAN_SPEED)	8	32h or 5Ah	R	[103:96]
card command classes	CCC	12	01x110110101b	R	[95:84]
max. read data block length	(READ_BL_LEN)	4	9	R	[83:80]
partial blocks for read allowed	(READ_BL_PARTIAL)	1	0	R	[79:79]
write block misalignment	(WRITE_BLK_MISALIGN)	1	0	R	[78:78]
read block misalignment	(READ_BLK_MISALIGN)	1	0	R	[77:77]
DSR implemented	DSR_IMP	1	x	R	[76:76]
reserved	-	6	00 0000b	R	[75:70]
device size	C_SIZE	22	00 xxxxh	R	[69:48]
reserved	-	1	0	R	[47:47]
erase single block enable	(ERASE_BLK_EN)	1	1	R	[46:46]
erase sector size	(SECTOR_SIZE)	7	7Fh	R	[45:39]
write protect group size	(WP_GRP_SIZE)	7	0000000b	R	[38:32]
write protect group enable	(WP_GRP_ENABLE)	1	0	R	[31:31]
reserved		2	00b	R	[30:29]
write speed factor	(R2W_FACTOR)	3	010b	R	[28:26]
max. write data block length	(WRITE_BL_LEN)	4	9	R	[25:22]
partial blocks for write allowed	(WRITE_BL_PARTIAL)	1	0	R	[21:21]
reserved	-	5	00000b	R	[20:16]
File format group	(FILE_FORMAT_GRP)	1	0	R	[15:15]
copy flag (OTP)	COPY	1	x	R/W(1)	[14:14]
permanent write protection	PERM_WRITE_PROTECT	1	x	R/W(1)	[13:13]
temporary write protection	TMP_WRITE_PROTECT	1	x	R/W	[12:12]
File format	(FILE_FORMAT)	2	00b	R	[11:10]
reserved	-	2	00b	R	[9:8]
CRC	CRC	7	xxxxxxxb	R/W	[7:1]
not used, always'1'	-	1	1	-	[0:0]

Table : The CSD Register Fields (CSD Version 2.0)

6.3.3 TAAC

This field is fixed to 0Eh, which indicates 1 ms. The host should not use TAAC, NSAC, and R2W_FACTOR to calculate timeout and should uses fixed timeout values for read and write operations.

6.3.4 NSAC

This field is fixed to 00h. NSAC should not be used to calculate time-out values.

6.3.5 TRAN_SPEED

The following table defines the maximum data transfer rate per one data line - TRAN_SPEED:

TRAN_SPEED bit	code
2:0	transfer rate unit 0=100kbit/s, 1=1Mbit/s, 2=10Mbit/s, 3=100Mbit/s, 4... 7=reserved
6:3	time value 0=reserved, 1=1.0, 2=1.2, 3=1.3, 4=1.5, 5=2.0, 6=2.5, 7=3.0, 8=3.5, 9=4.0, A=4.5, B=5.0, C=5.5, D=6.0, E=7.0, F=8.0
7	reserved

Table : Maximum Data Transfer Rate Definition

Note that for current SD Memory Cards, this field shall be always 0_0110_010b (032h) which is equal to 25 MHz - the mandatory maximum operating frequency of SD Memory Card.
In High-Speed mode, this field shall be always 0_1011_010b (05Ah) which is equal to 50 MHz, and when the timing mode returns to the default by CMD6 or CMD0 command, its value will be 032h.

6.3.6 CCC

The SD Memory Card command set is divided into subsets (command classes). The card command class register CCC defines which command classes are supported by this card. A value of 1 in a CCC bit means that the corresponding command class is supported.

CCC bit	Supported card command class
0	class 0
1	class 1
.....	
11	class 11

Table : Supported Card Command Classes

6.3.7 READ_BL_LEN

This field is fixed to 9h, which indicates READ_BL_LEN=512 Byte.

6.3.8 READ_BL_PARTIAL (always = 1 in SD Memory Card)

This field is fixed to 0, which indicates partial block read is inhibited and only unit of block access is allowed.

6.3.9 WRITE_BLK_MISALIGN

This field is fixed to 0, which indicates write access crossing physical block boundaries is always disabled in High Capacity SD Memory Card.

6.3.10 EAD_BLK_MISALIGN

This field is fixed to 0, which indicates read access crossing physical block boundaries is always disabled in High Capacity SD Memory Card.

6.3.11 DSR_IMP

Defines if the configurable driver stage is integrated on the card. If set, a driver stage register (DSR) shall be implemented

DSR_IMP	DSR type
0	no DSR implemented
1	DSR implemented

DSR Implementation Code Table

6.3.12 C_SIZE

This field is expanded to 22 bits and can indicate up to 2 TBytes (It is the same as the maximum memory space specified by a 32-bit block address.)
This parameter is used to calculate the user data area capacity in the SD memory card (not include the protected area). The user data area capacity is calculated from C_SIZE as follows: memory capacity = (C_SIZE+1) * 512K byte As the maximum capacity of the Physical Layer Specification Version 2.00 is 32 GB, the upper 6 bits of this field shall be set to 0.

6.3.13 ERASE_BLK_EN

This field is fixed to 1, which means the host can erase one or multiple units of 512 bytes.

6.3.14 SECTOR_SIZE

This field is fixed to 7Fh, which indicates 64 KBytes. This value does not relate to erase operation. Version 2.00 cards indicates memory boundary by AU size and this field should not be used.

6.3.15 WP_GRP_SIZE

This field is fixed to 00h. The High Capacity SD Memory Card does not support write protected groups.

6.3.16 WP_GRP_ENABLE

This field is fixed to 0. The High Capacity SD Memory Card does not support write protected groups.

6.3.17 R2W_FACTOR

This field is fixed to 2h, which indicates 4 multiples. Write timeout can be calculated by multiplying the read access time and R2W_FACTOR. However, the host should not use this factor and should use 250 ms for write timeout

6.3.18 WRITE_BL_LEN

This field is fixed to 9h, which indicates WRITE_BL_LEN=512 Byte.

6.3.19 WRITE_BL_PARTIAL

This field is fixed to 0, which indicates partial block read is inhibited and only unit of block access is allowed.

6.3.20 FILE_FORMAT_GRP

This field is set to 0. Host should not use this field.

6.3.21 COPY

Defines if the contents is original (=0) or has been copied (=1). The COPY bit for OTP and MTP devices, sold to end consumers, is set to 1, which identifies the card contents as a copy. The COPY bit is a one time programmable bit.

6.3.22 PERM_WRITE_PROTECT

Permanently protects the entire card content against overwriting or erasing (all write and erase commands for this card are permanently disabled). The default value is 0, i.e. not permanently write protected.

6.3.23 TMP_WRITE_PROTECT

Temporarily protects the entire card content from being overwritten or erased (all write and erase commands for this card are temporarily disabled). This bit can be set and reset. The default value is 0,i.e. not write protected.

6.3.24 FILE_FORMAT

This field is set to 0. Host should not use this field.

6.3.25 CRC

The CRC field carries the check sum for the CSD contents. It is computed according to Chapter 4.5. The checksum has to be recalculated by the host for any CSD modification. The default corresponds to the initial CSD contents.

6.4 RCA register

The writable 16-bit relative card address register carries the card address that is published by the card during the card identification. This address is used for the addressed host-card communication after the card identification procedure. The default value of the RCA register is 0x0000. The value 0x0000 is reserved to set all cards into the *Stand-by State* with CMD7.

6.5 DSR register (Optional)

The 16-bit driver stage register is described in detail in Chapter 6.5. It can be optionally used to improve the bus performance for extended operating conditions (depending on parameters like bus length, transfer rate or number of cards). The CSD register carries the information about the DSR register usage. The default value of the DSR register is 0x404.

6.6 SCR register

In addition to the CSD register, there is another configuration register named SD CARD Configuration Register (SCR). SCR provides information on the SD Memory Card's special features that were configured into the given card. The size of SCR register is 64 bits. This register shall be set in the factory by the SD Memory Card manufacturer.
The following table describes the SCR register content.

Description	Field	Width	Cell Type	SCR Slice
SCR Structure	SCR_STRUCTURE	4	R	[63:60]
SD Memory Card - Spec. Version	SD_SPEC	4	R	[59:56]
data_status_after erases	DATA_STAT_AFTER_ERASE	1	R	[55:55]
SD Security Support	SD_SECURITY	3	R	[54:52]
DAT Bus widths supported	SD_BUS_WIDTHS	4	R	[51:48]
reserved	-	16	R	[47:32]
reserved for manufacturer usage	-	32	R	[31:0]

The SCR Fields

SCR_STRUCTURE	SCR structure version	SD Physical Layer Specification Version
0	SCR version No. 1.0	Version 1.01-2.00
1-15	reserved	

Table : SCR Register Structure Version

• **SD_SPEC**

Describes the Physical Layer Specification Version supported by the card.

SD_SPEC	Physical Layer Specification Version Number
0	Version 1.0-1.01
1	Version 1.10
2	Version 2.00
3-15	reserved

Table : Physical Layer Specification Version

• **DATA_STAT_AFTER_ERASE**

Defines the data status after erase, whether it is 0 or 1 (the status is card vendor dependent).

• **SD_SECURITY**

Describes the Security Specification Version supported by the card.

SD_SECURITY	Security Specification Version
0	no security
1	Not used
2	Version 1.01
3	Version 2.00
4 .. 7	reserved

Table : SD Supported Security Algorithm

Note that it is mandatory for a regular writable SD Memory Card to support Security Protocol. For ROM (Read Only) and OTP (One Time Programmable) types of the SD Memory Card, the security feature is optional. In the case of Standard Capacity SD Memory Card, this field shall be set to 2 (Version 1.01). In the case of High Capacity SD Memory Card, this field shall be set to 3 (Version 2.00).

• **SD_BUS_WIDTHS**

Describes all the DAT bus widths that are supported by this card.

SD_BUS_WIDTHS	Supported Bus Widths
Bit 0	1 bit (DAT0)
Bit 1	reserved
Bit 2	4 bit (DAT0-3)
Bit 3	reserved

Table : SD Memory Card Supported Bus Widths

Since the SD Memory Card shall support at least the two bus modes 1-bit or 4-bit width, then any SD Card shall set at least bits 0 and 2 (SD_BUS_WIDTH="0101").

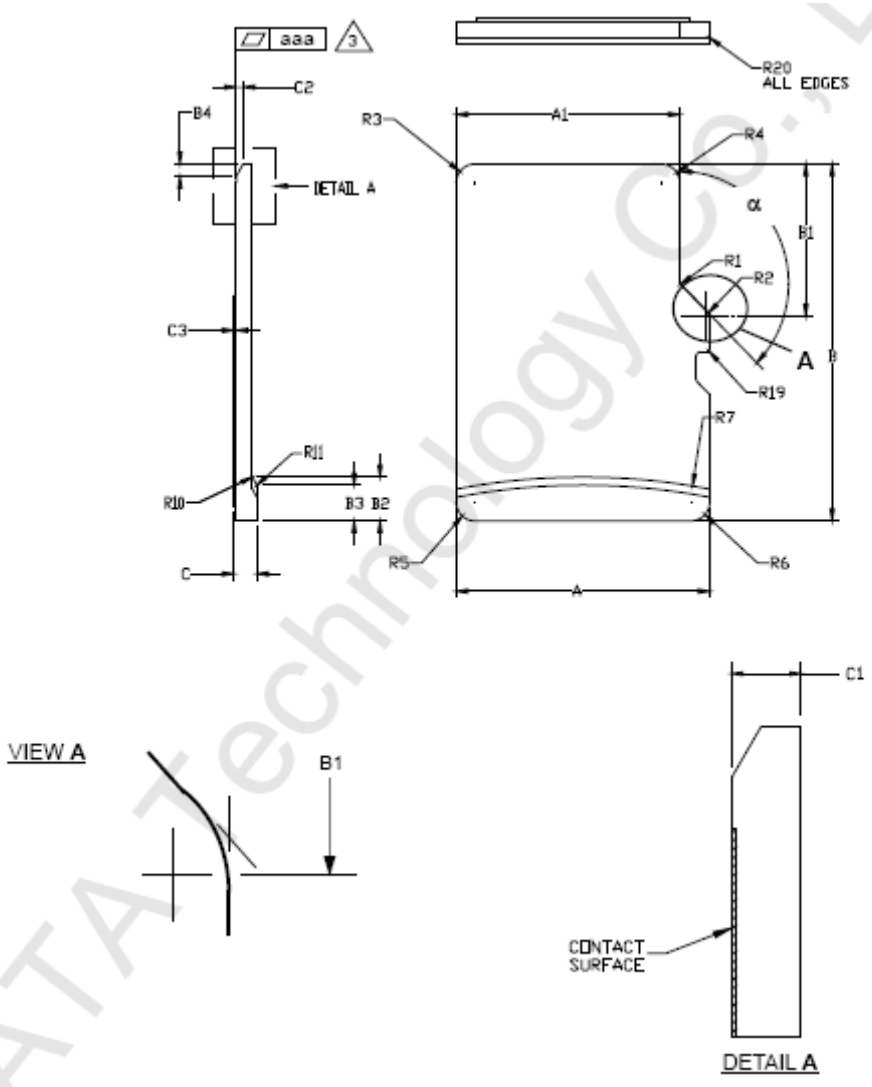
7. SPI Mode Introduction

The SPI mode consists of a secondary communication protocol that is offered by Flash-based SD Memory Cards. This mode is a subset of the SD Memory Card protocol, designed to communicate with a SPI channel, commonly found in Motorola's (and lately a few other vendors') microcontrollers. The interface is selected during the first reset command after power up (CMD0) and cannot be changed once the part is powered on.

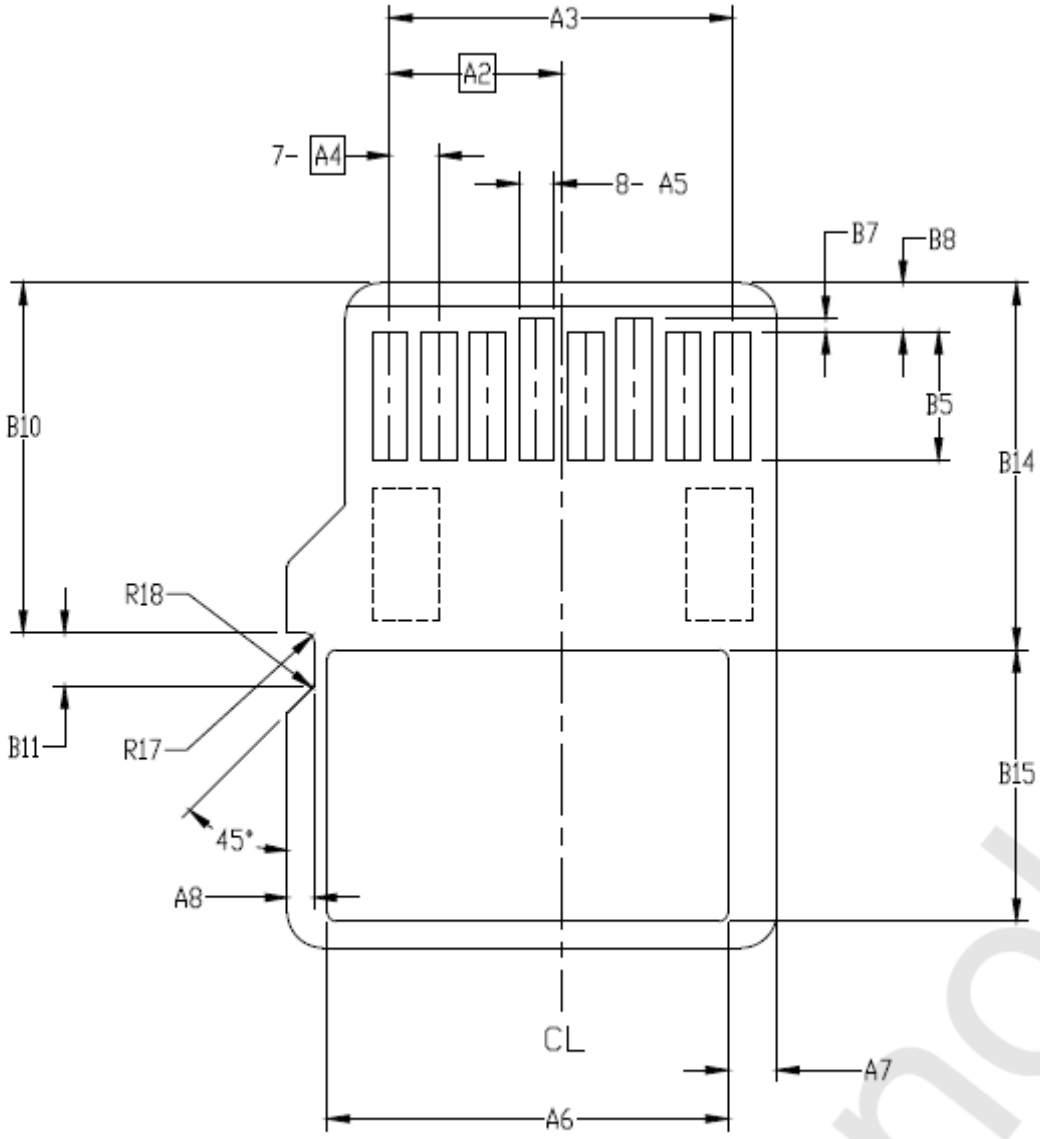
The SPI standard defines the physical link only, and not the complete data transfer protocol. The SD Memory Card SPI implementation uses a subset of the SD Memory Card protocol and command set. The advantage of the SPI mode is the capability of using an off-the-shelf host, hence reducing the design-in effort to minimum. The disadvantage is the loss of performance of the SPI mode versus SD mode (e.g. Single data line and hardware CS signal per card).

8. Mechanical Specifications and Appearance

Parameter	Description
Weight:	0.25g
Length:	11+-0.10mm
Width:	15+-0.10 mm
Thickness: Excluding Lip	1.0mm+-0.10mm

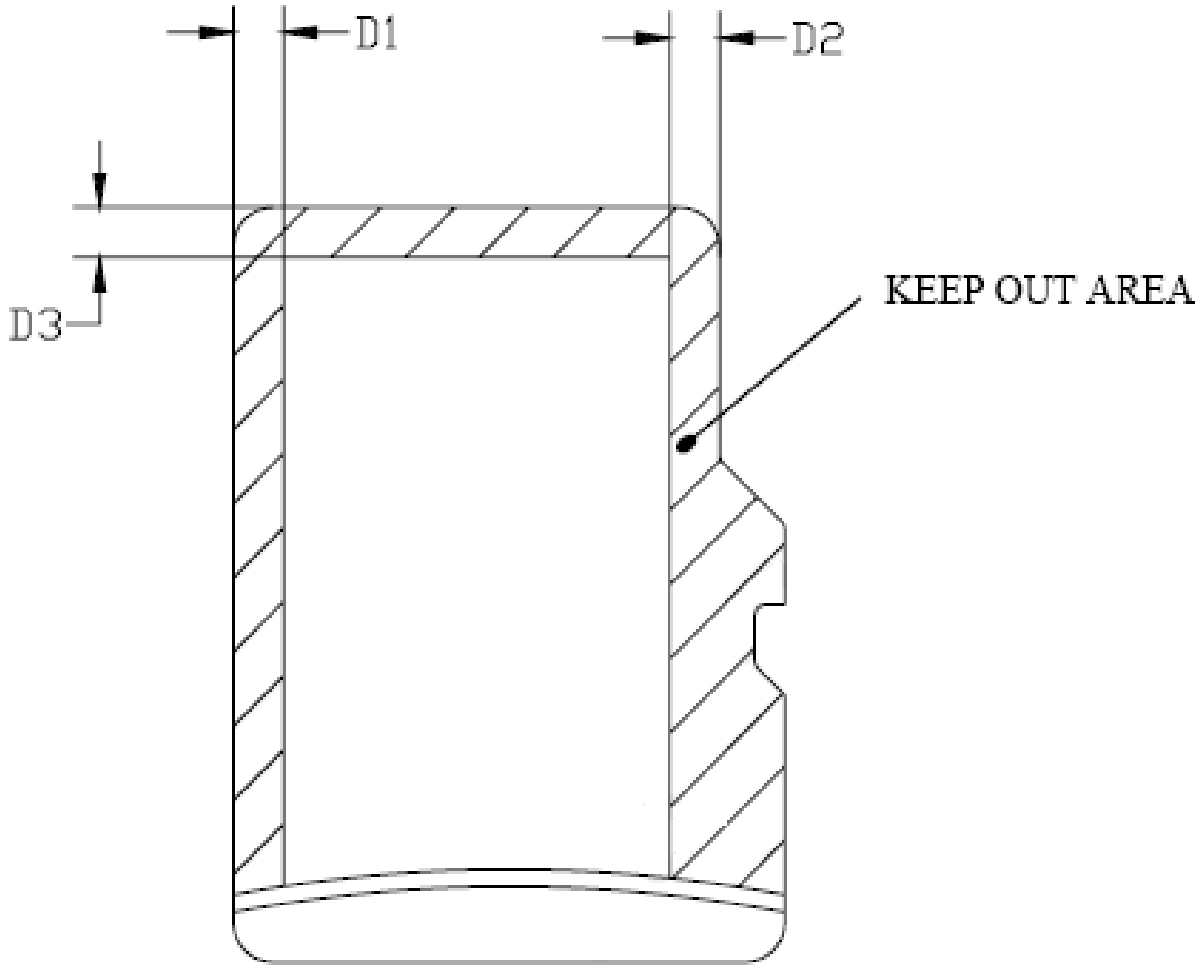


Mechanical Description: Top View



TYPE A: Recommended

Mechanical Description: Bottom View



Mechanical Description: Keep Out Area

	COMMON DIMENSIONS			
SYMBOL	MIN	NOM	MAX	NOTE
A	10.90	11.00	11.10	
A1	9.60	9.70	9.80	
A2	-	3.85	-	BASIC
A3	7.60	7.70	7.80	
A4	-	1.10	-	BASIC
A5	0.75	0.80	0.85	
A6	-	-	8.50	
A7	0.90	-	-	
A8	0.60	0.70	0.80	
A9	0.80	-	-	
A10	1.35	1.40	1.45	
A11	6.50	6.60	6.70	
A12	0.50	0.55	0.60	
A13	0.40	0.45	0.50	
B	14.90	15.00	15.10	
B1	6.30	6.40	6.50	
B2	1.64	1.84	2.04	
B3	1.30	1.50	1.70	
B4	0.42	0.52	0.62	
B5	2.80	2.90	3.00	
B6	5.50	-	-	
B7	0.20	0.30	0.40	
B8	1.00	1.10	1.20	
B9	-	-	9.00	
B10	7.80	7.90	8.00	
B11	1.10	1.20	1.30	
B12	3.60	3.70	3.80	
B13	2.80	2.90	3.00	
B14	8.20	-	-	
B15	-	-	8.20	
C	0.90	1.00	1.10	
C1	0.60	0.70	0.80	
C2	0.20	0.30	0.40	
C3	0.00	-	0.15	
D1	1.00	-	-	
D2	1.00	-	-	
D3	1.00	-	-	
R1	0.20	0.40	0.60	
R2	0.20	0.40	0.60	
R3	0.70	0.80	0.90	
R4	0.70	0.80	0.90	
R5	0.60	0.80	0.90	
R6	0.60	0.80	0.90	
R7	29.50	30.00	30.50	
R10	-	0.20	-	
R11	-	0.20	-	
R17	0.10	0.20	0.30	
R18	0.20	0.40	0.60	
R19	0.05	-	0.20	
R20	4	-	0.15	
α	133°	135°	137°	
aaa			0.10	

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